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ACQUISITION AND PROCESSING OF NEUTRON FLUX DATA FOR REACTIVITY EVALUATION

by

M. BERNEDE and L. STANCHI

1973

Joint Nuclear Research Centre
Ispra Establishment - Italy

Electronics Division

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ABSTRACT

The equipment has been designed for the acquisition of neutron flux data coming from a nuclear facility into a Laben 70 computer. Here a suitable program processes the data for evaluation of the reactivity. The instruments described herewith are a peripheral unit for the digital acquisition and an interface card which is directly inserted into the computer. All the equipment has been realized using monolithic integrated circuits. A particular synchronization logics for phasing the pulses corresponding to measurement time limits and to neutron flux is described.

KEYWORDS

REACTORS
NEUTRON FLUX
REACTIVITY
DATA ACQUISITION SYSTEMS
DATA PROCESSING
ELECTRONIC EQUIPMENT
DIGITAL COMPUTERS

ACQUISITION AND PROCESSING OF NEUTRON FLUX DATA FOR REACTIVITY EVALUATION

1. Introduction

The equipment has been designed for reactivity measurement in a nuclear reactor. This reactivity is evaluated from the measurement of a neutron flux detected by an ionization chamber. The measuring chain is indicated in fig. 1. The ionization chamber delivers at its output a current proportional to the incoming neutron flux. An electrometric amplifier with manually selected gain presents at the input of a voltage to frequency converter a variable voltage of suitable amplitude. The voltage range is adjusted to have the maximum frequency of 1 MHz for the maximum expected neutron flux. Finally a discriminator-shaper delivers a pulse succession with a rate proportional to the neutron flux.

The pulses are counted during a preset time and elaborated in a Laben 70 computer by a program(*) which processes the data for obtaining the requested information on the reactivity. An interface card conceived for the program-interrupt mode has been realized and inserted directly within the computer. The measuring time is in general prefixed butthe program is self-adjustable on the most suitable time as a function of the reactivity variations.

The minimum time (base-time) is prefixed as 40 ms. This allows to have a maximum number of pulses of 40,000 for the maximum rate so that the number can be stored in a 16-bits binary counter which is consistent with the 16 bits word of the computer. The base-time can be multiplied by a binary factor 2^n ranging between 2^0 and 2^{15} so that the time can be varied from 40 ms to about 22 minutes. The program is planned for adjusting the exponent n in correspondence to the variations of the neutron flux. The manual intervention of the operator on the amplifier gain gives under

(*) Developed by H.J. Metzdorf, Physics Division.

certain circumstances a more suitable matching of the voltage to frequency converter in respect of the experiment conditions. A future improvement can be the use of an amplifier whose gain is controlled by the computer so that a large range of neutron fluxes can be acquired without any intervention of the operator.

2. General description

A quartz oscillator of 13,107,200 Hz drives a series of binary dividers up to a frequency of 25 Hz corresponding to the base-time of 40 ms. A further frequency divider allows to multiply - as we said - the times by a binary factor. In this case if the time is not properly chosen the number of pulses arriving at the instrument during the measuring time could be higher than the maximum content of a 16 bits word (65,536). This can be avoided in two different manners :

1) The counter has four additional bits which are used as an overflow counter. The overflow bits are sent to the computer via the status word.

2) The pulse rate is divided by the same binary factor "n" as the time multiplier so that the maximum allowable count is 40,000 for any measuring time.

The experiment requires successive measurements without dead time and with a time uncertainty not greater than about a tenth of a microsecond. For that a quartz clock of about 13.1 MHz has been used.

The pulses to be counted and the time limits are completely uncorrelated so that it is necessary to be sure that when the data are transferred the binary counters are firmly set-up. For this purpose a suitable synchronizing logics is used. By that logics each incoming pulse is associated with another pulse which is controlled by the clock out of phase in respect of the pulses used to limit the measuring time and to reset the counters.

The instrument contains four scalers as seen in fig. 2. A first scaler is used to obtain a clock time of 40 ms (base-time) which is sent to a binary divider controlled by 4 bits for obtaining the measuring time. The same bits control also the pulse divider which divides (if not bypassed) the number of the incoming pulses by the same factor n. The random pulses are counted in a 20 bits counter after synchronization.

3. Synchronizing logics

The synchronizing logics has the purpose to arrange according to the following sequence : a) the incoming pulses b) the transfer command corresponding to the end of the measuring time c) the reset of the counters.

- pulse C (last recorded pulse in any measuring time)
- pulse TR (transfer of data corresponding to the elapsed time)
- pulse CL (reset of the pulse counters and frequency dividers)
- pulse C (first counted pulse in any measuring time)

The phase between TR and CL could be easily synchronized with a delay consistent with the set-up times. The phase between C and TR must be carefully controlled in order that the set-up time of the pulse counter is completed before the transfer. For that reason also pulse T corresponding to the end of the measuring time is transformed by the synchronizing logics in a pulse TR which has the appropriate phase in respect of a recorded pulse.

Two pairs of flip-flops (fig.3) are used for synchronizing the pulses C_p corresponding to the neutron flux and the pulses T corresponding to the end of the measuring time. The phases of the pulses used for the acquisition into the computer are controlled by the quartz clock indeed. The conditions under which the flip-flops swing are indicated in fig. 4 where two different time occurences of neutron pulses in respect of the transfer time are displayed. The output pulses are obtained by fourfold AND's as indicated by the expressions in fig. 4. The operation of flip-flops A_t , B_t and A_c , B_c is as follows. Two binary dividers produce two square-waves of frequency m and 2 m which control the phases of the transitions by conditioning flip-flops A's and B's. The cycle corresponding to an incoming pulse is indicated at the bottom of fig. 4 and initiated by the pulses for timing (T) and for counting (C_p) which reset flip-flops B_t and B_c respectively. Each cycle will be completed when the condition A = 0 and B = 1 is reached again. Only external events can initiate a new cycle by resetting B flip-flops with the asynchronous entry while the other three steps of the cycle are synchronously driven by the clock controlled by the interlaced conditions as indicated.

When the measuring time is elapsed, pulse T announcing the end of the time resets flip-flop B_t and initiates the complete cycle of the two flip-flops which will produce the transfer pulse TR which in turns is

responsible of the acquisition into the computer. The phase of TR in respect of two possible pulses is clearly apparent from the figure. A reset pulse CL is also generated which clears the frequency divider and the 20 bits pulse counter. A 20 bits register on the interface card is driven by the same pulse TR which warns the computer that the time is elapsed by calling for a program-interrupt. The logics contained in the interface card is quite normal for the used computer and will not be described. The time between the effective front of pulse C and the effective front of pulse TR is one clock and it is sufficient to allow the complete settling of the 20 bits ripple-through-carry synchronous TTL counter. The pulse divider and the clock divider are never cleared. The former must not be reset for statistical reason, the latter is not reset because unnecessary.

The indetermination time results to be one cycle of flip-flop m because a pulse can be phased in one cycle or in the next (see A_c or A'_c in fig. 4) but the time duration is recurring without any appreciable variation.

4. Operation

During routine measurements the time intervals recur all equal and the recorded number of pulses is acquired by the computer which starts a subroutine after the program-interrupt call. The subroutine contains normally an input instruction for data (INA or INM) an output instruction for a command register containing the bits forming the exponent "n" (WCA or WCM) and an instruction of read status (RSA or RSM). The status word gives the computer auxiliary information about the effective duration of the elapsed time (40 ms x 2^n where n = 0,1, ..., 15) and the eventual overflow of the pulse counter. The 16 bits of the status word have the significance reported in the table below

0 - control flag
1 - n.u. (not used)
2 - flag
3 - OF8 (overflow bit, weight 8)
4 - not ready
5 - n.u.
6 - n.u.

7 - n.u.
8 - n.u.
9 - AS1 (actual register status, time bit weight 1)
10 - AS2 (" " " " " " 2)
11 - AS4 (" " " " " " 4)
12 - AS8 (" " " " " " 8)
13 - OF1 (overflow bit, weight 1)
14 - OF2 (" " " 2)
15 - OF4 (" " " 4)

By that the computer is always ascertained during the data processing between the succeding transfers TR (minimum time 40 ms) of the status of the peripheral unit during the elapsed measurement.

Should the time be changed this must not affect the running measurement. For this purpose a particular register, called NEXT REGISTER, is provided. This register is driven by the command word from the computer (via WCA instruction) or by a manual command and can be set in any moment (fig. 5). This register will not act directly and gives only the conditions for a second register, called ACTUAL REGISTER, which will be set by the end of read status instruction. ACTUAL register drives a 1 of 16 decoder which provides the enabling signals E_0 , E_1, ... E_{15} for the exponent "n" applied to pulse and frequency dividers. NEXT register can be operated as said also by manual control provided that this command is enabled by a key operated switch. It is to be noted that during a measurement (e.g. a long time measurement) the status of NEXT register can be changed successively by the computer or by manual control. The action on ACTUAL register will be carried out by the last executed variation, i.e. the condition which will be found on NEXT register by the end of read status.

The logics throughout the instrument is made with conventional monolithic integrated circuits. As there are no particular problems of speed, DTL instead TTL circuits are normally used for exploiting the advantages of greater noise immunity, fan-in extension and wired-OR possibilities.

The peripheral unit contains four binary counters as seen in Fig. 2. Two of them are simply ripple-through counters and only the "frequency divider" and the "20 bits counter" are synchronous counters. The latter is a ripple-through-carry synchronous counter realized with TTL circuits for reasons of speed. The former is simply a DTL ripple-through-carry synchronous counter. The reason to be synchronous resides in the fact that due

to the long set up time in a ripple-through counter there should be phase errors when a time changement is operated, so that the first cycle with a new time could result shorter than necessary.

The pulse divider is shown in fig. 7. As no problems of speed are encountered, it is a simple ripple-through counter. Due to statistical reasons this counter can never be cleared. The clock divider is similar to the pulse divider.

Both the frequency divider and the 20 bits counter are cleared by the reset pulse CL produced by the synchronizing logics.

The outputs from the pulse divider and the frequency divider are taken four by four as a wired-OR and sent to two different fourfold OR's (fig.6 and 7). One of each set of 16 AND's for the exponent "n" is enabled by the condition stored in the 1 of 16 decoder. The outputs from 16-fold OR's are differentiated and sent to the synchronizing logics.

In fig. 8 a "Power on" circuit is indicated. This circuit resets the counters when the instrument is energized. It is based on the different thresholds between a combination of zener diode with a transistor and a DTL or a TTL circuit and has the peculiar feature to be independent of the rise time constant of the power supply.

5. Conclusion

The instrument is in operation at the ECO facility and constitutes a simple experimental mean for reactivity measurements. The digital acquisition instrument which follows the discriminator-shaper is realized in a two units Esone plug-in module. The interface card is directly inserted into the computer. Discrete Esone-TTL or TTL-Esone adaptors are used in inputs and outputs. The used technique is now a bit old and is made of monolithic IC's. All the logics used throughout the equipment is a positive one but in the transmission the complements are used for evident reasons. In fig. 9 the "Not ready" circuit is shown which gives a signalization interrupt to the computer when the peripheral is not connected or not energized. The input of a DTL or a TTL circuit is sinked by the peripheral only if the connection is made and if the peripheral is energized. The transmitted condition is $\overline{\text{READY}}$ in agreement with the general convention to transmit the complements.

In fig. 10 the peripheral unit is shown together with the interface card.

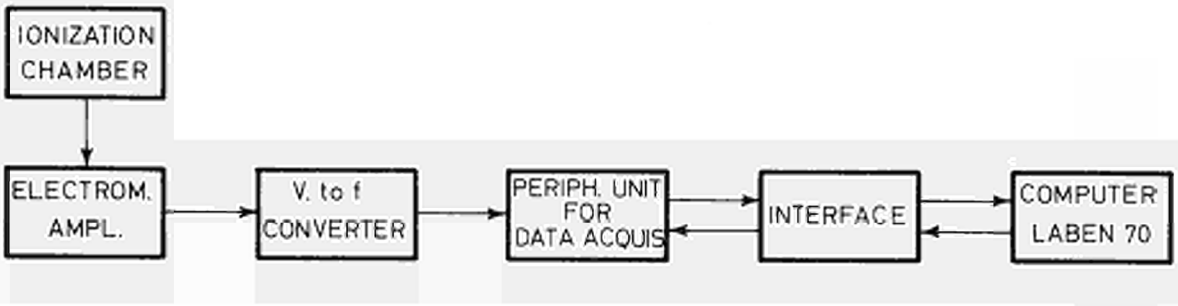

IONIZATION CHAMBER
ELECTROM. AMPL.
V. to f CONVERTER
PERIPH. UNIT FOR DATA ACQUIS
INTERFACE
COMPUTER LABEN 70

FIG. 1

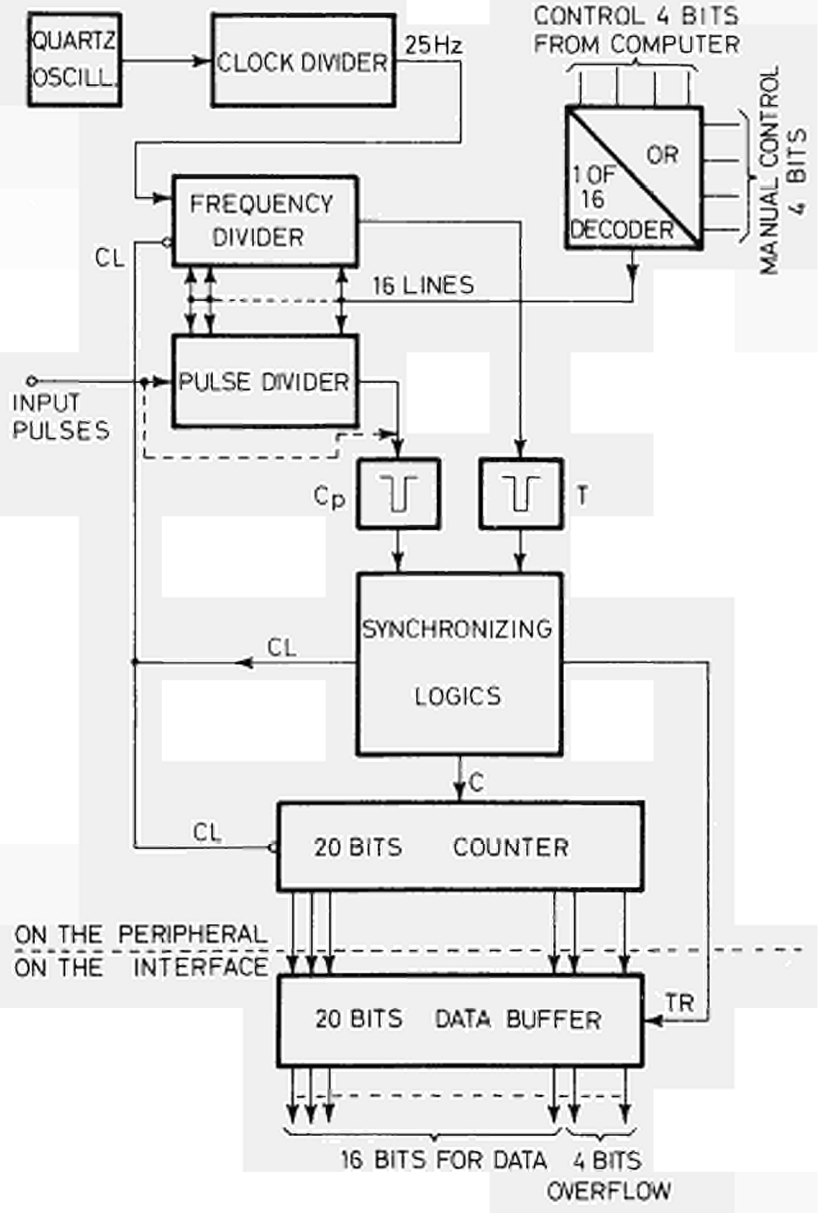

QUARTZ OSCILL.
CLOCK DIVIDER
25Hz
CONTROL 4 BITS FROM COMPUTER
OR
1 OF 16 DECODER
MANUAL CONTROL 4 BITS
FREQUENCY DIVIDER
CL
16 LINES
PULSE DIVIDER
INPUT PULSES
Cp
T
SYNCHRONIZING LOGICS
CL
C
CL
20 BITS COUNTER
ON THE PERIPHERAL
ON THE INTERFACE
20 BITS DATA BUFFER
TR
16 BITS FOR DATA
4 BITS OVERFLOW

FIG. 2

SYNCHRONIZING LOGIC

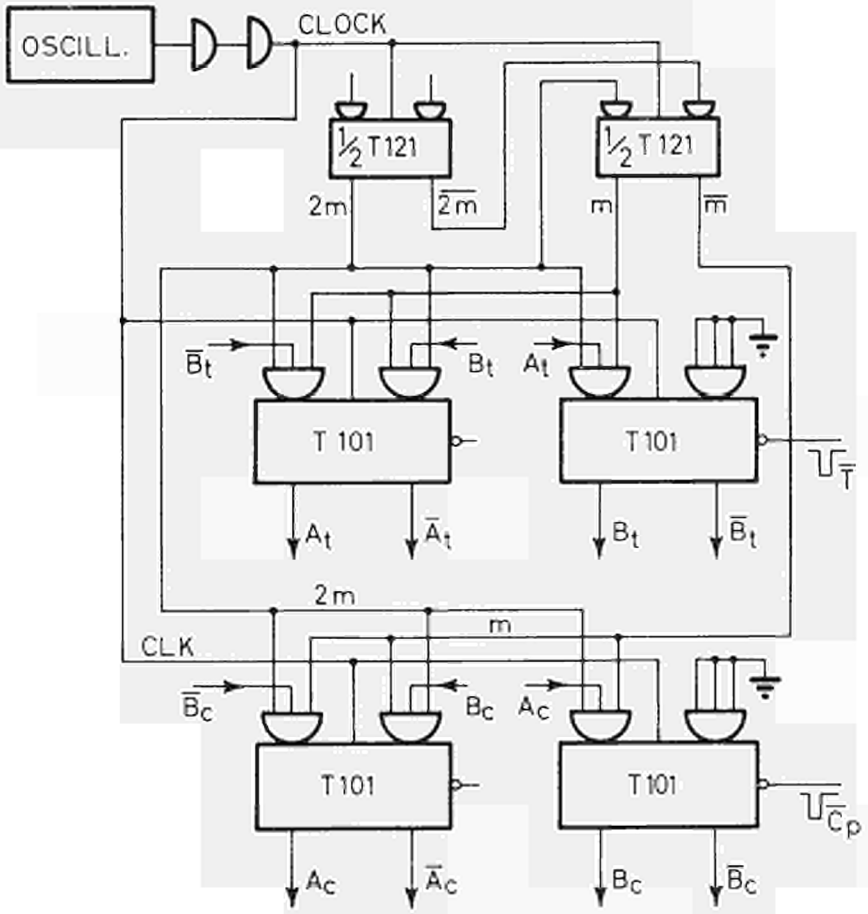
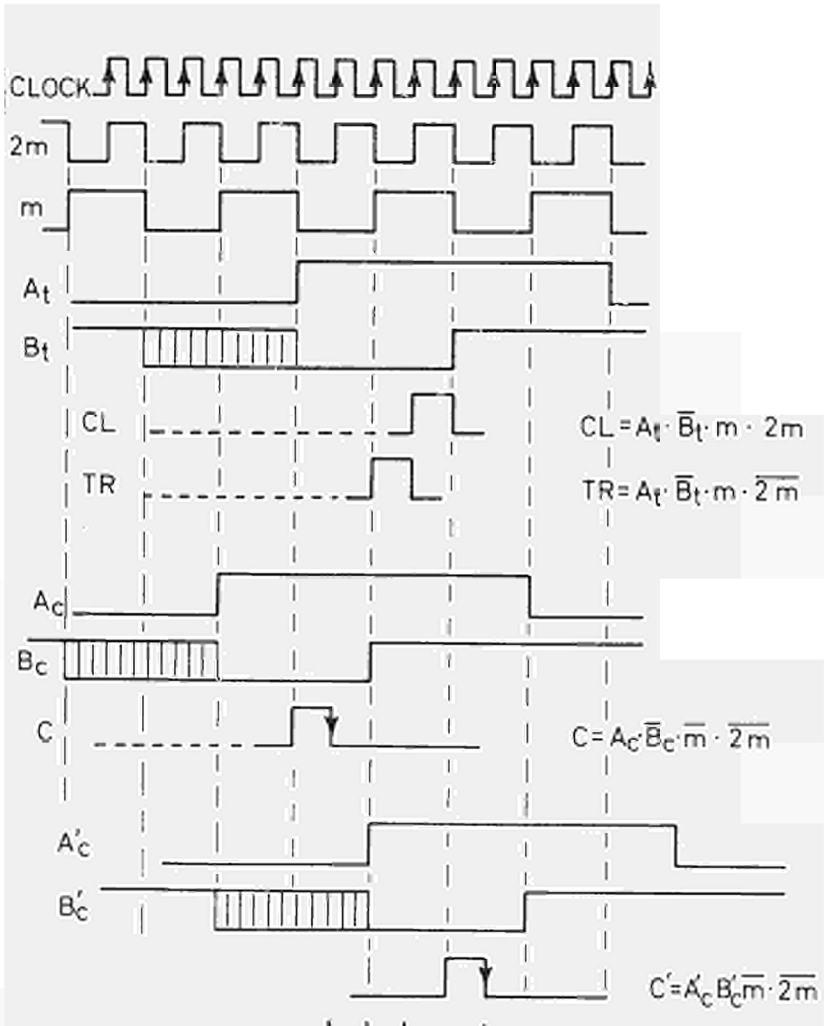


FIG. 3



ACTION TIME .....

C TR CL C

A	B
0	1
0	0
1	0
1	1
0	1

SET $A = \overline{B}$ { SET $A_t = CLK \cdot m \cdot 2m \cdot \overline{B}_t$; SET $A_c = CLK \cdot \overline{m} \cdot 2m \cdot \overline{B}_c$

RESET A=B { RESET $A_t = CLK \cdot m \cdot 2m \cdot B_t$; RESET $A_c = CLK \cdot \overline{m} \cdot 2m \cdot B_c$

SET B=A { SET $B_t = CLK \cdot m \cdot 2m \cdot A_t$; SET $B_c = CLK \cdot \overline{m} \cdot 2m \cdot A_c$

RESET B_t & B_c = EXT. EVENT

FIG. 4

FIG.4

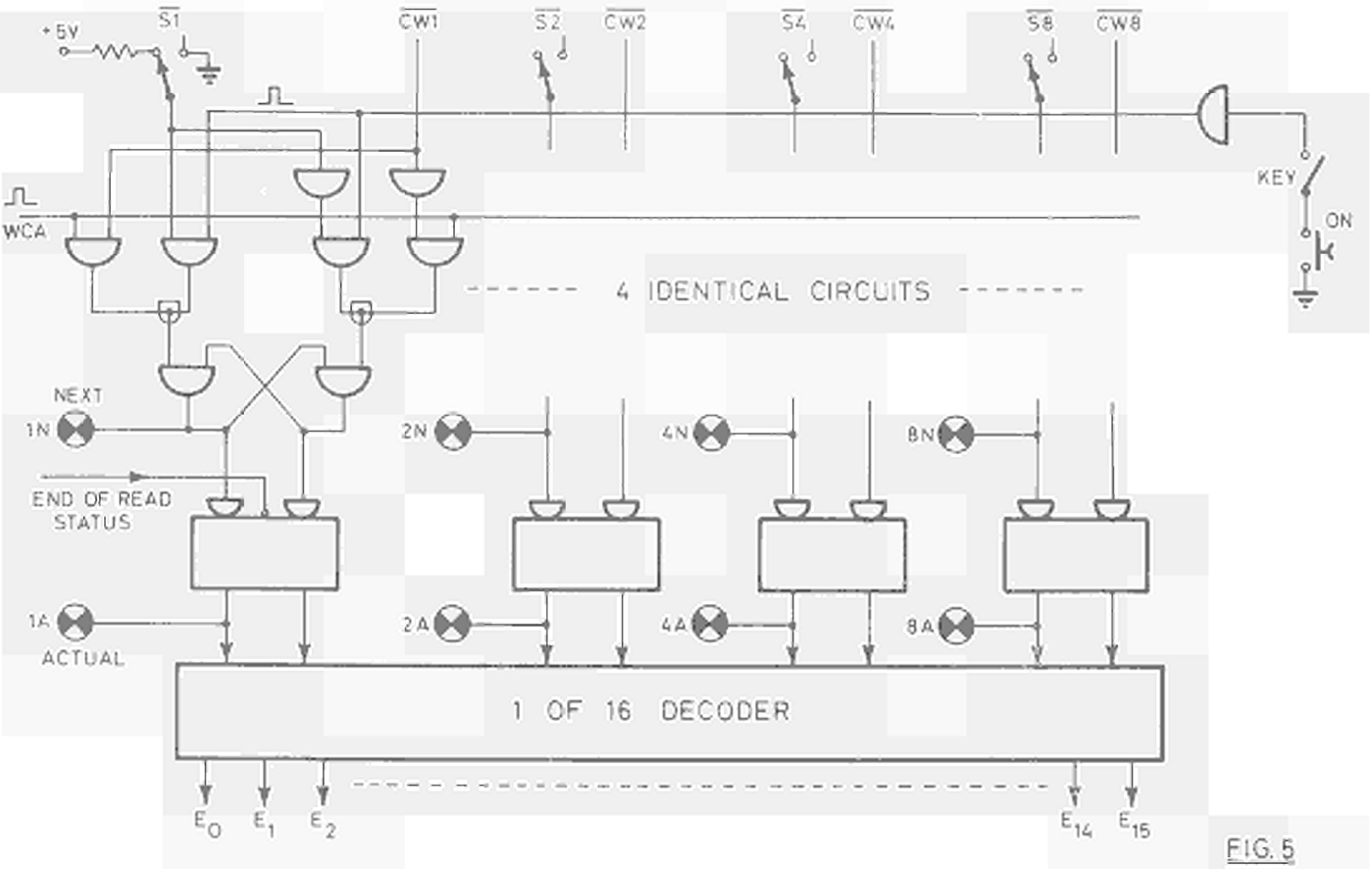


FIG. 5

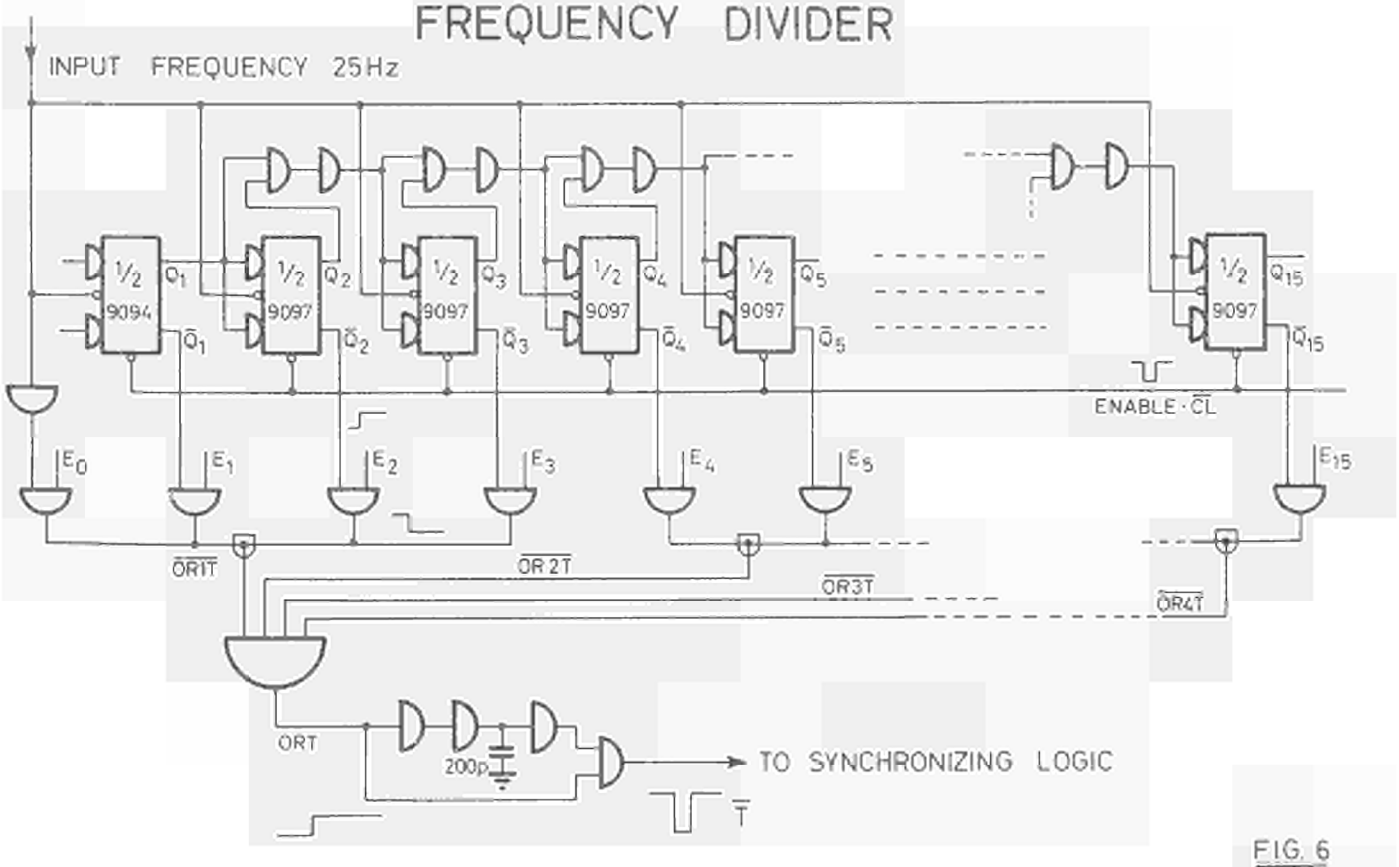


FIG. 6

PULSE DIVIDER

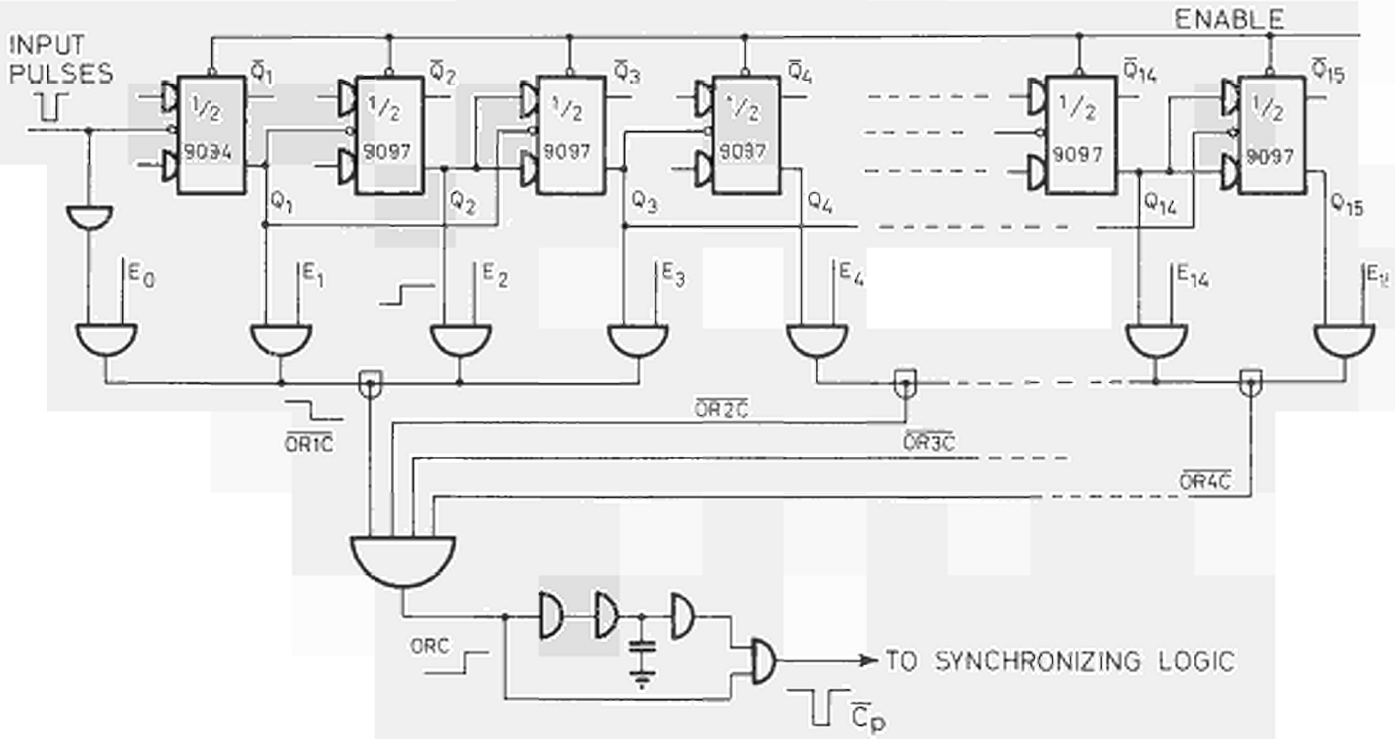


FIG. 7

"POWER ON" CIRCUIT

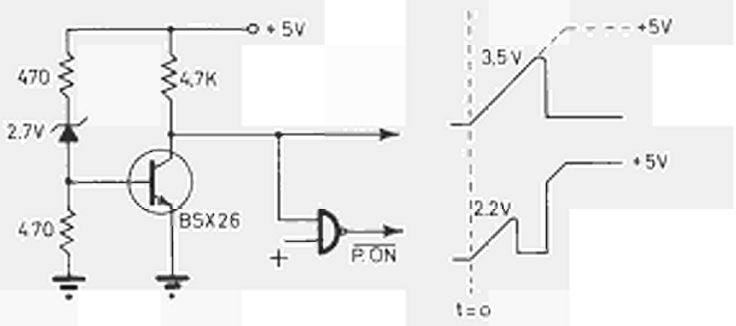


FIG. 8

NOT READY CIRCUIT

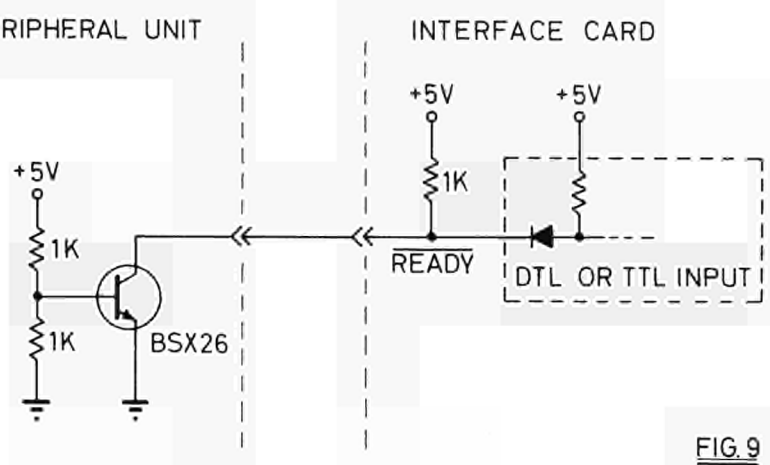
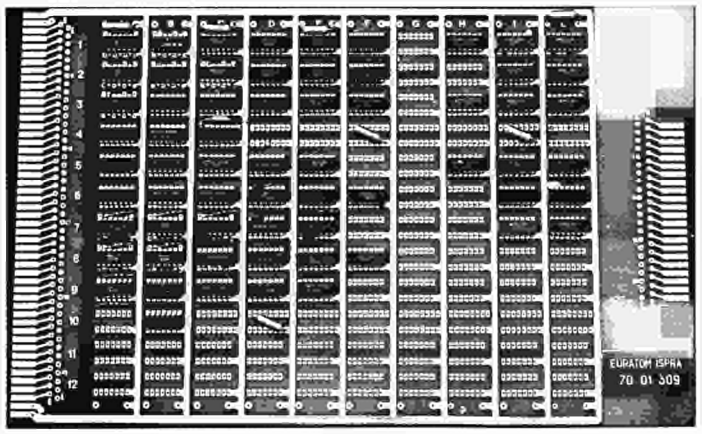


FIG. 9

FIG. 10



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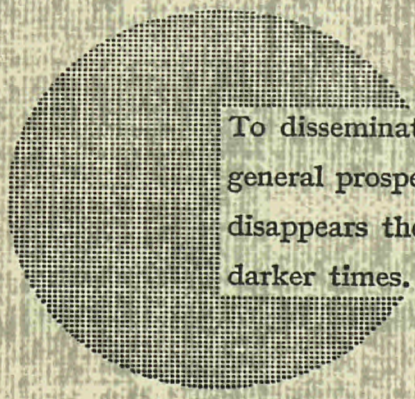

To disseminate knowledge is to disseminate prosperity — I mean general prosperity and not individual riches — and with prosperity disappears the greater part of the evil which is our heritage from darker times.

Alfred Nobel

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