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EUROPEAN ATOMIC ENERGY COMMUNITY - EURATOM

COUNTERS COUNTING IN ANY CODE

by

M. COMBET

1967



Joint Nuclear Research Center Ispra Establishment - Italy

Technology

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European Atomic Energy Community - EURATOM Joint Nuclear Research Center Ispra Establishment (Italy) Technology Brussels, February 1967 - 26 Pages - 7 Figures - FB 40

This paper describes a simple method for designing a sequential network. Provided a sequence of numbers, written by binary code, the method allows to design the corresponding circuit made of JK flip-flops.

Four examples are given for some sequences, one of which for a decimal counter.

An extension to ripple-through counters is applied to decimal counters, too.

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CONTENTS

.

INTRODUCTION	1
THE JK FLIP-FLOP	3
EXAMPLE I - COUNTER 0,2,3	5
EXAMPLE I - COUNTER 1,7,3,4,8,14,11	8
EXAMPLE III - COHERENT DECIMAL COUNTER	12
EXAMPLE IV - RIPPLE-THROUGH DECIMAL COUNTER	15
BIBLIOGRAPHY	18
APPENDIX I - EXAMPLE II	19
APPENDIX II - EXAMPLE III	22
APPENDIX III - EXAMPLE IV	24

SUMMARY

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This paper describes a simple method for designing a sequential network. Provided a sequence of numbers, written by binary code, the method allows to design the corresponding circuit made of JK flip-flops.

Four examples are given for some sequences, one of which for a decimal counter.

An extension to ripple-through counters is applied to decimal counters, too.

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COUNTERS

COUNTING IN ANY CODE +

Introduction

A counter is a device which can store a number of events (pulse for instance); every time an event occurs, the store number increases of 1.

The digits of this number are written in binary form for the counter is built with flip-flops which are binary elements.

A correspondence table for every set of digits (called number) and the "number value" has to be given: this table is called "code".

The problem is the following: having a sequence of numbers, we want to design the counter.

When the code is simple (binary, decimal, etc.) the circuit will be easy to design, but for general cases, it is necessary to use some formal method for computing the input conditions of the flip-flops 1, 3 given by the equation

$$X_{q} = f_{1}Q + f_{2}Q.$$

The following graphical method allows to separate more easily the functions f_1 (set) and f_2 (clear) when JK flip-flops are used. It can be extended to the other types of flip-flops.

⁺Manuscript received on December 6, 1966

Such a type of counter may be very useful for controlling a sequential machine, avoiding the conventional circuit: counter and decoding matrix using lot of components.

In the following, a counter will be given a name as a sequence of decimal number: every decimal number will represent the positions of the flip-flops. For instance, when we speak of the "0, 2, 5 counter", we mean a set of 3 flip-flops working in the following sequence.

0 0 0 0 1 0 1 0 1.

Now, the reader will find four examples:

- the first one illustrates the method in a very simple case where no minimization is necessary;
- the second one, rather complicate, with another type of flip-flop, needs a Karnaugh's table;
- the third example is a decimal counter;

These first three counters are coherent: every flipflop is triggered at the same time.

- the fourth example shows an extension of the method to a decimal ripple-through counter where flip-flops can be triggered by the clock pulse or another flipflop.

The JK Flip-flop

We will use the JK flip-flop type, because it is now the most generalized form of flip-flops of the integrated circuits.



Fig. 1: The JK flip-flop

A JK flip-flop has two outputs A, A and 3 inputs called S (set), C (clear) and CK (clock).

The flip-flop changes its state only when it receives a negative step on its input CK.

If the inputs S and C are different, the output A becomes the same as S after the clock pulse.

If S = C = 0, the flip-flop changes: the output at the n + 1 time becomes the complement value of that it had at the n time.

$$A_{n+1} = A_n$$

If S = C = 1, the flip-flop does not change, and

$$A_{n+1} = A_n$$

Finally, we have:

S	C	^A n+1
0	1	0
1	0	1
1	1	An
^{~~} 0	0	A _n .

Now we can see that in every case, we have two possibilities for controlling a flip-flop.

For instance, if we have

$$A_n = 1$$

and we want to have

 $A_{n+1} = 0$

we can take either

S = 0 C = 1or S = 0 C = 0.

Therefore, it will be necessary to put S = 0, but the input C will not be determinated.

.

Example I - Counter 0, 2, 3

Let us suppose now, we want to design a counter giving the following sequence:

Position	a	<u>b</u>
1	0	0
2	0	1
3	1	1

From the position 3, the counter will return to the position 1.

a) Let us write the 2 possible conditions of S_a and C_a for every position of the flip-flop a.

Position	8 	S _a	с _а
1	0	0 1	1 1
2	0	1 O	0 0
3	1	0 0	1 0
1	0		

This matrix may be reduced to:

Position	a	S _a	Ca
1	0	-	1
2	0	_	0
- 3	1	0	-

 $\mathbf{S}_{\mathbf{a}}$ having only one determinated position, we will take

 $S_a = 0.$

Position	Ծ	C _a
. 1	0	1
2	1	0
3	1	-

If we take $C_a = 0$ in the position 3, we will have

b) Let us do the same for the b flip-flop:

Position	<u>ъ</u>	S _b	с _ъ
1	0	1 0	0 0
2	1	1 1	0
3	1	0	1 0
1	0		

The reduced matrix is now:

Position	Ъ	s _b	С _р
• <u>••••••••••••••••••</u> •	-		
1	0	-	0
2	1	1	-
3	1	0	-

If we take $S_b = 1$ in position 1, we have

$$S_h = a$$

and C_b having only one position well determinated, we take

 $C_{\rm b} = 0.$

The schema of the counter will be:



Fig. 2: 3 positions coherent counter.

For this case, the selection of the conditions C_a and S_b was very simple. In general cases, Karnaugh's table will be necessary for taking the minimized form as we will see in the following example. Example II - Counter 1, 7, 3, 4, 8, 14, 11

Let us make up another example of sequence with another type of flip-flop, slightly different of the preceding one: for the complementation we must put 1 on both inputs S and C.

This case is that of conventional flip-flop, made with PNP transistors and working in negative logic, controlled by two And gates with two inputs, one of them receiving the clock pulse.



Fig. 3: Transistorized flip-flop

The equations of such a flip-flop are:

S _	<u>с</u>	^A n+1
0	1	0
1	0	1
1	1	An
0	0	A _n

Now let us take the sequence 1, 7, 3, 4, 8, 14 and 11 and let us try to find the best way for organizing a counter following such a sequence.

The sequence written in binary, will be:

Pos.	Decimal Value	a	<u>b</u>	<u>c</u>	<u>d</u>
1	1	1	0	0	0
2	. 7	1	1	1	0
3	3	1	1	0	0
4	4	0	0	1	0
5	8	0	0	0	1
6	14	0	1	1	1
7	11	1	1	0	1

Let us write directly the normal and reduced matrixes for a:

Pos.	<u>a</u>	S	Sa		
1	1	1 0	-	0	0
2	1	1 0	-	0 0	0
3	. 1	0 1	-	1 1	1
4	0	0 0	0	1 0	-
5	0	0 0	0	1 0	-
6	0	1 1	1	0 1	-
7	1	1 0	-	0 0	0
1	1				

The research of the simplest form for C_a and S_a will be made with the following Karnaugh's table:

		Sa							
ab cd	00	01	11	10	ab	00	01	11	10
Cu									
00	-	—	-		00		(1	0
01	0	-			01			0	-
11	_	1	_	_	11	_			
10	0	_	_]	—	10		_	0	
	•								

The simplification method consists of making groups of 2, 4, 8 ... adjacent "ones"; the bigger is the group, the simpler is the form of the result.

The cases where the function does not take a definite value, can be filled with 1 or 0, corresponding to the best way of simplification.

The complete method can be found in reference 2.

In our case we have:

$$S_a = b$$

 $C_a = bcd.$

The same computation has been made for b, c and d and can be found in Appendix I.

Finally, we have:

$$S_{a} = b \qquad C_{a} = bcd$$

$$S_{b} = c \qquad C_{b} = c$$

$$S_{c} = a + d \qquad C_{c} = 1$$

$$S_{d} = a \qquad C_{d} = a$$

and the corresponding schema will be:

- 10 -



Example III - Decimal counter with JK flip-flops

Now, we shall use four JK flip-flops in a decimal sequence:

Pos.	<u>a</u>	<u>b</u>	c	<u>d</u>
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

We see immediately that the a function is always complemented from any position to the following one.

Then:

$$S_a = C_a = 0.$$

Let us write the matrix for b:

Pos.	b 	S	с _ъ		
0	0	0 1	-	1 1	1
1	0	1 O	-	0 0	0
2	1	1 1	1	0 1	-
3	1	0 0	0	1 0	-

Pos.	<u>b</u>	S	S		
4	0	0 1	-	1 1	1
5	0	1 0	-	0 0	0
6	1	1 1	1	0 1	-
7	1	0 0	0	1 0	-
8	0	0 1	-	1 1	1
9	0	0 1		1 1	1
0	0				

The corresponding Karnaugh's table for ${\rm S}_{\rm b}$ and ${\rm C}_{\rm b}$ will be:

		Sb					Сь		
ab cd	00	01	11	10	ab cd	00	01	11	10
00		1	0		00	1		_	0
01	_	_			01	1	-		1
11	_				11			_	_
10		1	0	_	10	1			0

and we have

S_b ≖ a C_b = a + d The simplest form of the Boolean functions S_c , C_c , S_d and C_d can be found in the same way (see Appendix II). Finally, we have: $S_a \neq 0$ $S_b = a$ $S_b = a + b$ $S_c = a + b$ $S_d = a$ $C_c = a + b$ $C_d = a + b + c$ and the corresponding schema will be:



Fig. 5: Decimal counter with OR gates This schema can be transformed into NOR gate.



Fig. 6: Decimal counter with NOR gates

Example IV - Decimal ripple through counter

We shall work always with JK flip-flop. In that case, the CK inputs may be fed by the clock-pulse generator or the outputs of the other flip-flops: more possibilities are given and we can think the corresponding circuit will be simpler.

A clock-pulse coming from an output of a flip-flop will take place for the transition from 1 to zero.

Now we can list the clock-pulse available in a decimal counter:

					Avi	aila	ble	clo	<u>ck-</u>]	puls	e		
Pos.	<u>a</u>	b	<u>c</u>	<u>d</u>	Generator	<u>a</u>	<u>a</u>	b	<u>b</u>	<u>c</u>	<u>c</u>	d	<u>d</u>
0	0	0	0	0	+		+						
1	1	0	0	0	+	+			+				
2	0	1	0	0	+		+						
3	1	1	0	0	+	+		+			+		
4	0	0	1	0	+		+						
5	1	0	1	0	+	+			+				
6	0	1	1	0	+		+						
7	1	1	1	0	+	+		+		+			+
8	0	0	0	1	+		+						
9	1	0	0	1	+	+						+	

Let us take the b digit as we did in example III.

The clock-pulses for this flip-flop are necessary only when it will change its state: that is for the 1, 3, 5 and 7 positions (Nec CK).

We can take the output a as a clock-pulse, then it gives pulses at the 1, 3, 5, 7 and 9 positions (a CK).

Therefore, we must inhibit the 9th position (instead of the 0, 2, 4, 6, 8 and 9th positions for a coherent counter).

The S and C functions will not have determinated value for the 0, 2, 4, 6 and 8th position, that explains the more simple form of the corresponding Boolean function.

Pos.	Ъ	Nec CK	a CK	8 ,		С ^р	
		فنحمد معيرة مراه كرنج	······	*****		•••••	
0	0						
1	0	+	+	1 0	-	0 0	0
2	1				-		-
3	1	+	+	0 0	0	1 0	
4	0						-
5	0	+	+	1 0	-	0 0	0
6	1				-		-
7	1	+	+	0 0	0	1 0	-
8	0				-		-
9	0		+	0 1		1 1	1
0	0						

The matrix for the b output is:

We have:

s_b = 0

and the C_h Karnaugh's table will be:



 $C_b = d$

The computation for the c and d digits can be found in Appendix III.

 $\begin{array}{cccc} S_a = 0 & C_a = 0 \\ S_b = 0 & C_b = d \\ S_c = 0 & C_c = 0 \\ S_d = 0 & C_d = b + c. \end{array}$



Fig. 7: Decimal ripple-through counter with NOR gate

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<u>Appendix I</u> - Counter 1, 7, 3, 4, 8, 14, 11

1⁰) <u>FLIP-FLOP b</u>

Pos.	<u>b</u>	C_)
1	0	1 1	1	0 1	-
2	1	1 0	-	0 0	0
3	1	0 1	-	1 1	1
4	0	0 0	0	1 0	
5	0	1 1	1	0 1	-
6	1	1 0	-	0 0	0
7	1	0 1	-	1 1	1
1	0				



S_b=ē

C_b= c

2⁰) <u>FLIP-FLOP c</u>

Pos.	<u>c</u>	s	<u> </u>	<u>с</u>	<u> </u>
1	0	1 1	1	0 1	
2	1	0 1	-	1 1	1
3	0	1 1	1	0 1	-
4	1	0 1	-	1 1	1
5	0	1 1	1	0 1	-
6	. 1	0 1	-	1 1	1
7	0	0 0	0	1 0	-
1	0				



 $S_c = \overline{a} + \overline{d}$ $C_c = 1$

Pos.	<u>d</u>	S_d		C	<u> </u>
1	0	0 0	0	1 1	-
2	0	0 0	0	1 0	-
3	0	0 0	0	1 0	
4	0	1 1	1	0 1	
5	1	1 O	-	0 0	0
6	1	1 0	-	0 0	0
7	1	0 1		1 1	1
1	0				

ab cd	00	01	11	10	a b cd	00	01	11	10
00	[— _]	0	0	00	_	_	<u> </u>	
01		_ [_	01	0		1	_
11		_	-	_	11	_	0	-	-
10	1		0		10	_		<u> </u>	

S_d=ā

C_d=a

.

1⁰) <u>FLIP-FLOP c</u>

Pos.	c	S	S		
0	0	0 1	· _	1 1	1
1	0	0 1	-	1 1	1
2	0	0 1	-	1 1	1
3	0	1 0	5	0 0	0
4	1	1 1	1	0 1	-
5	1	1 1	1	0 1	-
6	1	1 1	1	0 1	-
7	1	0 0	0	1 0	-
8	0	0 1	-	1	1
9	0	0 1	-	1 1	1
0	0				



.

2°) FLIP-FLOP d

00

01

11

10

s_d = ā

	Pos.		<u>d</u>				s _d		Ca	. <u> </u>
	0		0			0 1	Ð		4 1	1
	1		0			0 1	-		1 1	1
	2		0			0 1	-		1 1	1
	3		0			0 1	· 🗕		1 1	1
	4		0			0 1	_		1 1	1
	5		0			0 1	-		1 1	1
	6		0			0 1	-		1 1	1
	7		0			1 0	· _		0 0	0
	8		. 1			1 1	1		0 1	-
	9		1			0	Ċ)	1 0	_
	0		0		-					
ab cd	00	01	11	10	ab cd]	00	01	11	10
00 0 1	-		-	_ 0	00 0 1		1	1	1	1



1⁰) <u>FLIP-FLOP c</u>

- - - -----

Pos.	c	Nec CK	b CK	Sc			Cc
0	0			-	-	-	-
1	0			-	-	-	-
2	0			-	-	-	-
3	0	+	+	1 0		0 0	0
4	1			-		-	-
5	1			-	-	-	-
6	1			-			-
7	1	+	+	1 0	0	1 0	-
8	0				Nacio		-
9	0			-	-	_	-
0	0						

 $S_c = C_c = 0$

÷

Pos.	d.	Nec CK	a CK	S	L		0 _d
0	0			-	-	_	_
1	0		+	0 1	-	1 1	1
2	0			-	-	-	-
3	0		+	0 1	-	1 1	1
4	0			-	-	-	-
5	0		+	0 1	-	1 1	1
6	0			-	-	-	-
7	0	+	+	1 0	-	0 0	0
8	1			-		-	-
9	1	+	+	0 0	0	1 0	_
0	0						





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Page	Ligne	Expression corrigée
1	20	$X_q = f_1Q + f_2\overline{Q}$
3	5	two outputs A, \overline{A}
3	15	$A_{n+1} = \overline{A_n}$
4	5	$\circ \circ \overline{A_n}$
6	8	$C_a = \overline{b}$
6	24	S _b = a
8	. 15	$1 1 \overline{A_n}$
10	10	$C_a = b \overline{c} \overline{d}$
10	14	$C_a = b\overline{c}\overline{d}$
10	15	$S_b = \overline{c}$ $C_b = \overline{c}$
10	16	$S_c = \overline{a} + \overline{d}$
10	17	S _d = a
13	avant-dernière	$S_b = \overline{a}$
13	dernière	$C_b = \overline{a} + d$
14	5	$S_{b} = \overline{a} \qquad C_{b} = \overline{a} + d$
14	6	$S_c = \overline{a} + \overline{b} C_c = \overline{a} + \overline{b}$
14	7	$S_d = \overline{a}$ $C_d = \overline{a} + \overline{b} + \overline{c}$
15	12	<u>Generator a a b b c c d d</u>
17	7	$C_d = \overline{b} + \overline{c}$
22	<u>ab 00 01</u>	<u>11 10</u> <u>ab 00 01 11 10</u>
	c d	c d
	$\begin{vmatrix} 0 & 0 \\ 0 & 1 \end{vmatrix} \begin{pmatrix} - \\ - \end{pmatrix} = \begin{vmatrix} - \\ - \\ - \end{vmatrix}$	- $ 0 0 1 1 0 1 1 0 1 1 0 1 1$
	10 1 1	0 1 10
23		<u>ab 00 01 11 10</u>
		c d

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Alfred Nobel

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