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DIGITAL COMPARATORS FOR HANDLING OF DATA FROM NUCLEAR EXPERIMENTS

by

F. COLLING

1966

Joint Nuclear Research Center
Geel Establishment - Belgium

Central Bureau for Nuclear Measurements - CBNM

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For data handling purposes two-state comparators should be preferred because of their possible simplicity and speed. A maximum flexibility in application is given, in addition.

Three state comparators, also by combination of two two-state comparators, can be used with advantage for regulation purposes as for instance gain stabilization.

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SUMMARY

Two digital comparators for binary or binary coded decimal information have been realized and tested. The comparator stages for all bits are cascaded and identical, so that they can be used as standard units in building block systems. The operation time of the 20-bit three-state transistor comparator is about 90 ns per bit for the slowest comparison. With a 10-bit window comparator, containing two two-state comparators with tunneldiodes as threshold elements, a minimum comparison speed of about 6 ns per stage (bit) was reached. This characteristic can be improved up to one order of magnitude, if necessary, when fast tunneldiodes are used.

For data handling purposes two-state comparators should be preferred because of their possible simplicity and speed. A maximum flexibility in application is given, in addition.

Three state comparators, also by combination of two two-state comparators, can be used with advantage for regulation purposes as for instance gain stabilization.

C O N T E N T S

LIST OF FIGURES

1. INTRODUCTION (°)

1.1. Some needs for a digital comparator in nuclear physics.

The analog signals from particle detectors will mostly be digitized in analog-to-digital converters. The further handling of the experiment information will therefore be done in a digital manner.

In order to attain adequate resolution, many bits will be required. Especially in multiparameter experiments, which are of increasing importance , the data words will be extremely long. As a consequence, big store capacities will be required. If such big stores are not available, one has to look for a compromise between the desired resolution, experiment time and instrumentation capabilities.

It will often happen, that only a smaller part of all channels (data words) are of real interest. If one could provide the physicist with a unit, which would permit the selection of one or more regions of interest, either the quantity of information or the number of bits per data word - to be stored - could be reduced.
A digital comparator is a unit which enables the selection of a region of interest. It will discriminate whether the information has a greater value than a selected number, or a smaller one. Two comparators combined to one unit will enable the user to select a window. In this manner, the quantity of information to be stored and handled may be reduced to a certain amount.

Comparators can also be used for the integration of selected parts of the spectrum. Besides a reduced quantity of information, one will also get a smaller number of bits at the cost of a decrease in resolution for that particular parameter, of which the parts are selected. In certain cases a unit with subtracting

(°) Manuscript received on March 15, 1966

properties should be used for the selection of a region of interest.
Maintaining the same resolution with a reduced number of bits would be the main advantage. To obtain a digital window, an additional comparator would be required. Particularly for experiments with on-line analysis, it can be of real advantage - or even a requirement - to have the disposal of a unit which allows a reduction of the number of bits per word.

For off-line experiments,on the other hand, a unit which reduces the quantity of information words to be stored, may also be useful.

It may be pointed out, that the application of a digital comparator will not by far be limited to the above mentioned goals. Besides the use as a selector of regions of interest, there will be other applications for data processing.

1.2. Basic function and way of operation of the digital comparator.

A digital comparator compares a digital data word (number X) to a digital programmed word (number A) and indicates whether the number X is greater than A, smaller than A, or equals A.

Generally, all available data words are compared with one programmed word during one data handling cycle. In some applications it may occur that one data word is compared to several programmed words.

In most cases, the number of stages of the comparator will at least be equal to the number of bits of the programmed word.

The comparison is effectuated as follows:
Each comparator stage compares the corresponding bits of A and X. Some stages detect equality of the applied bits, the other indicate unequality. The

conclusion of the comparison must be prescribed by the stage of highest significance of all stages detecting unequality.

1.3. Some general aspects of digital comparators.

Two- and three-state comparators have been realized for the comparison of digitized data.

A three-state comparator (1,2,4,5,6) is able to identify separately if a data word (X) is greater, equal or smaller than a programmed word (A).

In a two-state comparator (3,7), two of the three possible states are combined to one state and $X > A$ or $X \leq A$, $X < A$ or $X \geq A$, $X \neq A$ or $X = A$, can be identified. A unit with the latter mentioned property is known as an equality detector and is normally very simple in lay-out.

In most of the known comparators, the comparison process begins with a separate comparison of bits with the same significance. Concerning the detailed comparison procedure, i.e. in principle how to find out the most significant bit for which unequality is given and the way to elaborate the result, different solutions have been described (1 - 6).

In general a comparator should allow a symmetrical access of digital numbers to be compared. Special comparator types, in which the programmed word can be controlled only manually by means of mechanical switches or relays, are better characterized as digital thresholds (1,3). They are not very flexible in application, but can be very simple in lay-out.

In nuclear experiments, comparators have been used by different people, to reduce single parameters in multiparametric analysis to one data word (channel) with the aid of a digital window (1,2,3). The width and the location of the window in the parameter region

is fixed by the programmed words of two single comparators.

For the planned applications, which are more general, comparators should allow a high degree of flexibility. Needing only one comparator stage per data word bit seems to be the most suitable solution. The comparator stages are then identical for all bits, so that they can be used as standard units in a building block system. An improved version of such a proposal (6), which is a three-state comparator allowing automatic programming, if needed, has been realized by us and will be desribed. Another solution (7), a two-state comparator for which the same concept was applied, but simpler in lay-out and allowing greater processing speed, has been developed in addition. It is this latter type of comparator which meets our demands in the best way.

2. REALIZED COMPARATORS

2.1. Introductory considerations

Both realized comparators - a three-state comparator with transistors and a window comparator, consisting of two identical two-state comparators with tunneldiodes - comprise n similar cascaded stages (Fig. 1). The number of stages n is not limited for circuitry reasons; both the required quantity of components and comparison time are roughly proportional to the number of bits (n).

The following description is related to Fig. 1.
Each stage compares a bit of the data word (X) with the corresponding bit of the programmed word (A). Both words are supposed to be binary or binary decimal coded. The comparison result of one stage is determined either by the information delivered from the preceding stage, or by the configuration of the two applied bits.
The symbols x_i, a_i and c_i respresent the configuration of the "i"-th bit of the two compared words and of the

"i"-th comparator stage; x_n and a_n represent the most significant, x_o and a_o the least significant bits of X and **A**.

The result of the comparison of **A** and X may be available at the output of that comparator stage, corresponding either to the most or to the least significant bit (C_n or C_o). The latter is possible, if the most significant comparator stage detecting unequality will impose its result to all comparing units between that deciding stage and the output.

If the comparator output is at the most significant stage, the flow of decisive information will be from less significant stages to the most significant one (L.M. mode). The deciding comparator stage imposes then its result to more significant comparator stages, which all must have detected equality.

If the output of the comparator is at the least significant comparator stage, the flow of deciding information will go from a more significant to the least significant stage (M.L. mode). In this case the deciding comparator stage must impose its result to less significant comparator stages, which may have detected themselves unequality of both signs or equality.

In case both words **A** and X are equal, the single comparator stages do not influence each other; every stage produces an equality signal.

If all possible data words have the same probability of occurrence, the more significant comparator bits take the decision in the great majority of the comparisons (nearly 97 % of all decisions are taken by the 5 most significant bits out of 10). If the comparison process of a next data word would be started immediately after the result of the preceding comparison is available, the integral comparison time needed for a defined amount of data words will therefore be smaller for an L.M. mode than for an M.L. mode comparator. Both comparator types

will need about the same time, if the comparisons are initiated by clock pulses, because the fastest allowed repetition rate is given by the comparison needing the longest time to be effectuated.

The functional analysis of a comparator can be reduced to the examination of two consecutive stages R and S (Fig.2).

The signal R_{out} is the comparison result of the stage R, provided that the stage preceding it does not influence the comparison of $R(Q_{out} = 0)$. The symbols X_R, X_S and A_R, A_S represent the information delivered by two consecutive bits of the data word (X) and the programmed word (A). The comparison result of the two examined stages, S_{out}, is determined by the analog sum of the three input signals delivered to the stage S (R_{out}, X_S and A_S). According to the significance of the stage R, either the unequality signal R_{out} eliminates the influence of any configuration of X_S and A_S (M.L. mode), or R_{out} is eliminated by an unequality signal produced by X_S and A_S (L.M. mode). As either unequality decision ($X > A$ or $X < A$) can be caused by different combinations of the three input signals, their analog sum can reach different values, but the output signal must attain always a discrete level for the same decision. This can be realized by the introduction of a threshold device, delivering the required output level, if the sum of the input signals is greater than the threshold. The weight of the three input signals R_{out}, A_S and X_S must be chosen in such a way that for either unequality between A and X, their sum has the right value in relation to the threshold.

A three-state comparator stage needs two opposite thresholds. If neither threshold is reached, the comparator indicates equality of A and X.

A two-state comparing unit has only one threshold. The equality case and one of the unequality cases postulate

a driving signal smaller than the threshold, whereas for the opposite unequality case the sum of input signals must be greater than the threshold.

A three-state comparator can be realized also by an adequate combination of two two-state comparators.

2.2. Three-state comparator with transistors

2.2.1. General description

A three-state comparator has been built as a general study for the comparison of binary or binary coded-decimal information with up to 20 bit word length. All comparator stages are equal and contain two transistors as main elements. The realized comparator is identical in principle to a circuit given by others (6) but it requires only two supply voltages (± 6 V), which are in use as standard voltages for digital electronic equipment in our laboratories.

The required input signals and the delivered output signals are of the same "level"-type: a binary "one", "1" = + 5 V and a binary "zero", "0" = 0 V.

A data word (X) to be compared with the programmed word (A) is stored via read-in gates in a 20 bit binary register (Fig. 3). A buffer stage is used between the register and the comparator, allowing a greater fan-out for the connection of different comparators.

The programmed word can be controlled manually by means of twenty toggle switches, which allow to connect the "A" inputs of the comparator stages to a voltage of 0 Volts or - 4,3 Volts, respectively. The voltage of - 4,3 Volt is derived from the standard

power supply voltage of - 6 Volts with zener diodes.

On the circuit cards of the comparator, space was provided for an A- register and a suitable coupling stage, to allow an electronic control of the programmed word.

The three different comparison results $X > A$, $X = A$, $X < A$ are available at seperate outputs; for instance for "X > A", the voltage at the "X > A" output is: $U_S \approx + 5$ V and $U_S = 0$ at the other outputs.

The course of a comparison process can be explained with Fig. 3. An incoming clock pulse will first reset the X-register via an input logic unit. Then the X-word to be compared which is available at "read-in", is stored into the X-register via read-in gates with a "set" pulse. The "set" pulse has a fixed delay with respect to the "reset". After setting, the comparison begins and its result will be available for the realized comparator at the output of the least significant comparator stage (M.L. mode). The time necessary for a comparison depends on the words to be compared and on their number of bits. The maximum possible comparison time determines the delay between the clock pulse and a strobe pulse, which will sense the output logic unit in such a way, that the state of the least significant comparator stage is directed to the appropriate output. In addition the strobe pulse initiates a read out command. The time intervals, necessary for "reset", set, comparison and read out" determine the maximum clock pulse rate, which was about 500 kc/s for the realized comparator.

In the single comparator stages which are described more in detail in the following chapter, a phase inversion of signals occurs, caused by transistors in emitter-grounded configuration. This was taken into

account by using the complements of the corresponding bits for the comparison in the even numbered stages.

2.2.2. Description of a single comparator stage

The lay-out of one stage (S) preceded and followed by identical stages (R and T) is shown in Fig. 4. The stage R is connected to a more significant bit of the words to be compared ($R \equiv C_{i+1}$) and T to a less significant bit than S ($T \equiv C_{i-1}$). The comparison result is available at the comparator stage belonging to the least significant bit (M.L. mode).

The three states of the comparator stage representing the different possible results - $X > A$, $X = A$, $X < A$ - are realized by using two complementary transistors as a differential switch.
For an unequality between X and A, either transistor must be switched on, while the other one is in the cut-off state. In the given circuit and for $X > A$, the input signal S_{IN} must exceed a positive threshold voltage, $S_{IN} > U_{TH}$, to switch on the n-p-n transistor (T_1). The corresponding output signal (S_{out}) is of negative polarity, because of the phase inversion in the transistors which are used in emitter-grounded configuration. For $X < A$, S_{IN} has to overcome a negative threshold voltage, $|S_{IN}| > - U_{TH}$, to switch on T_2 and S_{out} will be positive. For equality between X and A, both transistors will be in the cut-off state, $|S_{IN}| < \pm U_{TH}$. The output signal of the unloaded stage will be zero, because of the symmetrical lay-out of the circuit.

The given conditions for the input signal of the stage S must be satisfied by the analog sum of the three input signals X_S, A_S and R_{out}, which may be defined as follows:

$X_S = U_{XS}$, if the "i"$^{-th}$ bit (x_i) of the data word is in the "1" state; U_{XS} is a positive voltage, equal for all comparator stages and it may be written: $X_S = +1$ ($\bar{X}_S = 0$) for x_i = "1", $X_S = 0$ ($\bar{X}_S = +1$) for $x_i = 0$.
$A_S = U_{AS}$, if the "i"$^{-th}$ bit of the programmed word (a_i) is in the "1" state and a negative signal will be delivered to the comparator stage S. U_{AS} is a negative voltage and it follows: $A_S = -1$ ($\bar{A}_S = 0$) for a_i = "1"; $A_S = 0$ ($\bar{A}_S = -1$) for $a_i = 0$.
The signal R_{out}, which is delivered by the preceding stage R, represents the comparison result of the more significant stages. If also here unity signals are taken for an easier explanation, R_{out} is a positive signal for $X > A$, i.e. $R_{out} = +1$; $R_{out} = -1$ if $X < A$ and $R_{out} = 0$, if $X = A$.

If the necessary predominant influence of R_{out} on the comparison result, for $R_{out} \neq 0$, is taken into consideration, one may write for the analog sum of input signals, which should determine S_{IN} :

$$S_{IN} = Z.R_{out} + X_S + A_S \qquad (1)$$

R_{out}, X_S and A_S are unity signals as stated before and Z is a factor, $Z > 1$.

In table I, the possible comparison conditions for the stage S are given. Two most critical conditions for a correct operation of the comparator can be defined with the results for S_{IN} in table I.

- The predominance condition; if the result of the preceding stages (R_{out}) is opposite with respect to the result of the stage S itself, R_{out} must have the greatest weight in order to determine the state of the stage S; for $(X > A)_R$ and $X_S < A_S$ or $(X < A)_R$ and $X_S > A_S$, table I indicates, $S_{IN} = Z-1$.

- The independence condition; if $R_{out} = 0$ and $X_S \neq A_S$, the signal X_S respectively A_S must not be influenced by the zero signal level delivered from the preceding stage R to the input of S, X_S or A_S have to determine the state of the stage S.

For the lay-out of a comparator stage, the quantitative behaviour of a transistor as threshold device must be taken into account. In case of an unequality decision, the threshold voltage U_{TH} must not only be exceeded; the transistor which is to be saturated will also draw a current I_b because of its limited current gain (β). The current, which is necessary to bring the transistor into the "on" state, will be: $I_{bmin} \approx U_{BE}/\beta.R_c$ and the corresponding overdrive factor is $K = I_b/I_{bmin}$. For reliable operation and sufficient speed of response, a minimum overdrive factor $K_{min} > 1$ should be assured and the minimum β of the used transistors has to be taken into account. However, the overdrive factor K will also influence the minimum time interval between two comparisons in another way. The greater K/β, the greater will be the base-emitter junction charge to be discharged in case of a change in the comparison state of a stage i.e. the minimum distance between two different comparisons increases with increasing K/β.

The maximum overdrive factor K_m will occur, if the same unequality for consecutive bits is given. $|S_{IN}| = Z+1$ and the greatest value of K_m will depend on the maximum current gain of the used transistors. The smallest possible value of the ratio K_m/K_{min} for this circuit can be found by calculations. ($K_m/K_{min} \approx 5$ for $R_D/R_c \geq 0{,}5$). This optimum value of the ratio guarantees a maximum speed of response.

The smallest value of K is given for the before mentioned most critical comparison conditions. For the predominance condition one obtains:

$$K_1 = \beta \cdot \left[\frac{m - 2(m+1)\varepsilon}{m(1+m)} - \frac{\delta + 2\varepsilon}{n} \right] \qquad (2)$$

with $m = \frac{R_D}{R_C}$; $n = \frac{R_B}{R_C}$; $\delta = \frac{U_{X_S}}{U_{BB}} = -\frac{U_{A_S}}{U_{BB}}$;

and $\varepsilon = \frac{U_{TH}}{U_{BB}}$,

and for the independence condition it is found:

$$K_2 = \beta \cdot \left[\frac{\delta - 2\varepsilon}{n} - \frac{2\varepsilon}{1+m} \right] . \qquad (3)$$

K_1 and K_2 have a minimum for $\beta = \beta_{min}$.

δ and ε of equations (2) and (3) are determined by the supply voltage conditions. δ is smaller than one, because buffer stages are used between the register and the comparator. Best driving conditions can be achieved with $K_1 = K_2 = K$. An overdrive factor of $K_{min} = 2$ seems to be necessary for a reliable operation. The maximum allowed value of ε can be calculated in function of m with K/β as parameter. (Fig. 5). As shown, the maximum value of ε that can be tolerated depends only to a limited extent on δ for which a minimum value, guaranteed by the transistor manufacturers, must be considered. The values of m and n should be kept as small as possible, in order to obtain high operation speed. The best values for m with $K/\beta = 0{,}1$ are $0{,}5 \leq m \leq 2$ for which ε_{max} varies between 0,08 and 0,095. The corresponding values of n can be calculated with equation (4), which follows from (2) and (3) (Fig. 6):

$$n = 2\delta \cdot \frac{1+m}{1 - \frac{2\varepsilon}{m}} \qquad (4)$$

For the used silicon transistors and the standard power supplies ($U_{BB} = \pm 6V$) a value of ϵ smaller than ϵ_{max}, was realized by using as threshold voltage the difference between the base-emitter saturation voltage and the diffusion voltage of biased germanium diodes in the emitters of the transistor pairs.

For a comparator, designed for operation in L.M. mode, ϵ can be greater, as shown in Fig. 7. The best values for m are: $1 \leq m \leq 3$ with $0,14 \leq \epsilon \leq 0,15$, $\beta = 20$ and $K = 2$. The corresponding values for n are given in Fig. 8.
A greater value of ϵ_{max} admits either smaller supply voltages - of interest for the realization of a comparator with integrated circuits - or greater threshold voltages U_{TH}.

The collector current of the saturated transistor can be chosen in a way to obtain maximum switching speed. The collector resistor is then fixed for a given supply voltage ($R_C \cong U_{BB}/I_C$) and R_B and R_D are determined by the factors n and m.

With the chosen circuit lay-out (Fig. 4) it was not necessary to select transistors. Reliable operation, also for the critical comparison conditions, was reached within a great temperature range because the threshold voltages of the comparator stages are largely independent on temperature. This is due to the mutual compensation of the temperature coefficients of the transistor base-emitter voltage and the diffusion voltage of the biasing diode.

2.3. A window comparator comprising two two-state comparators with tunneldiodes.

2.3.1. General description

The realized window-comparator consists of two identical

two-state comparators of ten stages each.

The data word (X) and both programmed words (A_1 and A_2) are stored in 10-bit binary registers.

If the window boundaries should be controlled only manually, the A-registers can be replaced by tumblers representing the two signal levels corresponding to the states of a binary bit.

Both two-state comparators will test whether $X > A_1$ (resp. A_2) or $X \leq A_1$ (resp. A_2). The lower (resp. upper) limit of the window is represented by A_1 (resp. A_2). The decisions of these comparators are fed to a logic unit, which will deliver a signal at only one of the three outputs, labelled "$X > A_2$", "$A_1 < X \leq A_2$" and "$X \leq A_1$".

All the required input signals and the delivered output signals are of the same "level"-type : "1" $\approx$ + 5 Volt; "0" $\approx$ 0 Volt and the used power supplies are in accordance with the ESONE rules (+6 Volts and -6 Volts).

The time needed for merely the evaluation of one 10-bit data word is smaller than 60 nanoseconds. The maximum comparison rate for the realized unit is limited to $5.\ 10^6$ words per second, because some additional time will be required for other purposes, as for instance the read-in of data.

The block diagram of the realized window-comparator is shown in Fig. 9. The time diagram for the different signals during one comparison cycle is represented in Fig. 10. The following description is related to both figures.

An incoming clock signal will initiate a comparison cycle. First of all the clock input gate will be

closed and the "busy"-signal appears at its output (S_4); at the same time the registers, both comparators and the three output binaries (B_1, B_2 and B_3) will be reset. After a time T_1 the numbers X, A_1 and A_2 are read-in into the appropriate registers by means of a common set-pulse. After ($T_1 + T_2$) the reset signal to both comparators will be removed, i.e. the actual comparison is started. Within 60 ns a comparison result will be available, preparing only one of the three output and-gates (G_1, G_2 or G_3). Then the strobe pulse passing the prepared and-gate will set the appropriate output binary (B_1, B_2 or B_3). The clock input gate will be opened again and the "busy-free" level will turn to "free". Until the next clock signal is given, the window-comparator conclusion (i.e. either $X > A_2$ or $A_1 < X \leq A_2$ or $X \leq A_1$) will remain available at the corresponding output (either S_1, S_2 or S_3).

2.3.2. Description of the circuit diagram of one single comparator stage

The circuit of a two-state comparator stage with a tunneldiode as threshold element is shown in Fig. 11. According to the bistable behaviour of a tunneldiode, the reset position can be characterized with a binary value "0", for which the low voltage state should be prefered in our case. Thus "reset" = binary "0", means $U_{TD} < U_{peak}$ and "set" = binary "1", means $U_{TD} > U_{valley}$. Because of the low resistivity of the tunneldiode, it may be characterized as a current sensitive element. In order to set the tunneldiode, a current $I_{TD} > I_{Peak}$ must be available. Once in the "set"-position, a stage may be forced to deliver current to its neighbouring stages, if these are in the reset state. In order to avoid that

a set stage will return under such conditions to the low voltage state, due to a lack of current, a bias current $I_M > I_V$ is supplied to each stage.

As it can be seen from the circuit diagram (Fig. 11), the current through the tunnel diode will be determined by the three possible input signals, i.e. on one hand X_S and A_S from the corresponding X- and A-bits and on the other the signal R_{out}, delivered by the preceding stage (R). The significance of these three signals must be determined in accordance to the working principle of the comparator. If the stage S detects unequality, it will be set (S_{out} = "1") for $X_S > A_S$; for $X_S < A_S$ the stage will remain in the reset position (S_{out} = "0"). S_{out} has the value "1" only for X > A, because the realized comparator is of the "X > A" type. According to the L.M.-mode of operation of this comparator, a signal from the preceding less significant stage (R_{out}) may only contribute to the comparison result of the stage S, if the stage S detects equality.

Summarizing the above mentioned conditions :
For $X_S > A_S$: S_{out} must be "1", independent of R_{out}.
For $X_S < A_S$: S_{out} must be "0", independent of R_{out}.
For $X_S = A_S$: S_{out} can be determined by R_{out}.

With table II it is shown that the given comparison conditions can be fulfilled if the X-bit and the complement of the A-bit ($\bar{A}$) are fed to the two bit-inputs of each stage. (For an "X < A" type comparator, $\bar{X}$ and A should have been applied.) This necessity follows from the fact that a comparison is equivalent to a simplified subtraction. It is to be performed, for an X > A comparator, by adding to the minuend (X) the complement of the subtrahend ($\bar{A}$) and the eventual carry pulse from a preceding less significant stage

(R_{out}). The sum will be greater "1", i.e. a carry signal (S_{out} = "1") is produced, only if at least two of the three possible signals are present. The sum itself is neglected.

The given conditions for digital signals must be transformed into analog input currents for the tunnel diode. With the symbols in Fig. 11 one may write:

$$I_X = \frac{U_X}{R_B} \; ; \quad I_A = \frac{U_A}{R_B} \; ; \quad I_{Rout} = \frac{U_o}{R_o} \; .$$

U_o is the mean voltage difference between a set and a reset tunnel diode. The signals should be chosen equal to allow maximum tolerances for the elements of the comparator, i.e., $I_X = I_A = I_{Rout} = I_s$. (6)

The already mentioned biasing current I_M ($I_M > I_V$) and the signal current I_S can be determined in relation to the peak current (I_P) of the tunnel diode. The tunnel diode must not be set if one input current I_S is delivered, i.e.:

$$I_M + I_S < I_p \; ; \tag{7}$$

on the other hand, the tunnel diode must be set if at least two signals I_S are present, i.e.:

$$I_M + 2 I_S > I_p \; . \tag{8}$$

In order to allow maximum tolerances for I_S and I_p, one should select the maximum no-trigger signal ($I_M + I_S$) and the minimum trigger signal ($I_M + 2 I_S$) symmetrical to the peak current. It therefore follows from equations (7) and (8):

$$I_p - (I_M + I_S) = (I_M + 2 I_S) - I_p$$

or

$$I_S = \frac{2}{3} (I_p - I_M). \tag{9}$$

For the selected tunnel diode (AEY 11, I_p = 5mA ± 5%) a minimum value of six is guaranteed for the quotient of the peak- and valley currents. If one chooses for safety reasons $I_M = 1{,}5\ I_V$, it follows for I_M with

$I_V = I_p/6$,

$$I_M = I_p/4 \qquad (10)$$

and for I_S with (9) and (10)

$$I_S = I_p/2 \qquad (11)$$

For the used tunnel diode one finds: $I_M = 1.25$ mA, $I_S = 2.5$ mA.

A reset current I_{RES} is required, before a new comparison can begin. This current must be greater than the maximum possible tunnel diode current, i.e.:

$$-I_{RES} > 2\,I_S + I_M = 5/4\,I_p \qquad (12)$$

For safety reasons it was chosen, $-I_{RES} = 1.5\,I_p \cong U_{BB}/R_R$

2.3.3. Tolerance considerations of the circuit lay-out

The allowed tolerances for the signals of a comparator stage and its elements follow from the critical comparison conditions mentioned above and were analyzed for a stage S.

For a maximum no-trigger signal, $(I_M + I_S)$, the tunneldiode should remain in the reset state. Such conditions are given for the stage S if: $X_S < A_S$, $X_R > A_R$ and the stage preceding R also in the set position. The signal $I_{Rout} = I_S$ delivered to the stage S, will have its maximum value for a maximum U_o of the stage R because of element tolerances. Worst case conditions may occur if in addition, the peak current of the tunneldiode in the stage S will be lower than its mean value.

A minimum trigger signal $(I_M + 2I_S)$ to set the stage S, is given for $X_S = A_S$, $X_R > A_R$ and the stage preceding R in the low voltage state. Then the set stage R must deliver to its preceding and to its following stage (S) a signal I_S which will be lower than

the mean value because of the load condition of **R**. Worst case conditions may be given if the peak current of the tunneldiode in stage **S** is higher than its mean value and U_{valley} of the stage **R** has its minimum value because of element tolerances.

If the set stage **S** ($X_S > A_S$) has to deliver two signals I_S to its neighbouring stages **R** and **T** ($X_R < A_R$, $X_T = A_T$) the tunneldiode of stage **S** could be reset because of overload if I_M is smaller than I_V. However, this is improbable because the time necessary to switch a tunneldiode to the high voltage state is shorter than the switching time for the inverse direction. As soon as the tunneldiode of T has reached the high voltage state, the stage S has to deliver only one signal I_S.
The tolerances of the used elements are:

$$I_p = 5\text{mA} \pm 5\% \; ; \; \frac{1}{I_p} \cdot \frac{\Delta I_p}{\Delta t} \leq -2.10^{-3}/°C$$

$$U_F = 470\ \text{mV} \pm 10\ \%; \quad \frac{\Delta U_F}{\Delta t} \leq -2\ \text{mV}/°C$$

(U_F = tunneldiode forward voltage for $I_{TD} = I_p$).
The resistance tolerances are given with ± 5 %, and variations of the "set" voltage U_o were smaller than ± 15 % for the possible load conditions of a stage.

Calculations have shown, that for a supply voltage variation of ± 1 % and an ambient temperature between + 10 °C and + 40 °C, the safety distances of the signals from I_{peak}, 25 % under ideal conditions, are reduced to 6 % of I_p.

3. Measurements and tests

For both comparators the security margins of the

discussed worst case comparison conditions and the maximum comparison time were measured. An integral operation test controlling the faultless working of both comparators for temperature and supply voltage variations, was carried out by determining the maximum comparison rate. The maximum clock rate will be lower to a certain extent because of the limited speed of the associated electronic circuitry for logic operations.

3.1. The three-state transistor comparator

To control the critical comparisons, the minimum overdrive factors for the predominance and the independence comparison conditions (K_1, K_2) were determined by measuring the corresponding base currents in all comparator stages. The lowest values of K/β which were found are:

$$\frac{K_1}{\beta} = \frac{I_{B1}}{I_c} \simeq 0{,}15 \; ; \quad \frac{K_2}{\beta} = \frac{I_{B2}}{I_c} \simeq 0{,}13$$

i.e. for the minimum current gain, β min = 20, it follows:

$$K_{1min} = 3 \quad \text{and} \quad K_{2min} = 2{,}5$$

The maximum overdrive factor (K_m), which occurs when two consecutive stages have detected the same unequality, can also be determined from the maximum measurable base current,

$$\frac{K_m}{\beta} = \frac{I_{bm}}{I_c} \simeq 0{,}66$$

i.e. for $\beta_{max} = 100$, $\quad K_{max} = 66$.

The maximum time necessary for a comparison will be measured when all heavily saturated transistors are driven into cut-off, i.e., the same unequality decision

being detected on all stages, and the next decision gives equality of all compared words. The time interval from the begin of such a comparison (X = A) up to the moment at which the result is available at the comparator output was 1.8 µs, i.e. about 90 ns per stage.

3.2. The two-state tunneldiode comparator.

On both two-state comparators of the window comparator, the same tests were performed separately.

For the critical comparison conditions, mentioned under 2.3.3., the minimum differences between the tunneldiode current (I_{TD}) and the tunneldiode peak current were measured for all stages.
The security margin of I_{TD}, which avoids a forbidden setting of a tunneldiode, was found to be $(I_P-I_{TD})_{min}$ = 6 % of I_p. The minimum excess current to set a tunneldiode was found to be $(I_{TD}-I_P)_{min}$ =7 % of I_P.

A too important undershoot of the reset pulse could have introduced an erratic setting of a stage. For the realized comparator, the undershoot was not greater than 3 % of I_{peak}. Therefore a correct operation also under worst case conditions could be assured.

The maximum time needed for a comparison can be measured if the decision of the least significant tunneldiode has to be transmitted to the output, because all more significant stages detect equality of the applied bits. The time elapsed from the begin of such a comparison up to the moment the result was available at the most significant stage output, is about 60 ns; i.e., about 6 ns per stage.

3.3. Integral operation test.

Both comparators were tested under identical operational conditions. An equal probability for all possible data words in one test interval was realized by using the data word register as a scaler (Fig. 12), i.e. in one scaler cycle all data words ($0-2^{n-1}$) occured only once. For a complete test of the comparators, 2^n test cycles would have been necessary to compare all possible programmed words with all data words. However, the manually controlled programmed words were set in such a way that the correct operation of the critical comparison conditions of each comparator stage could be checked in n+1 tests.
Special care was taken to measure only during complete scaler cycles, and with an auxiliary scaler, the number of cycles in one test interval could be fixed.

For temperatures between 20 and 45°C and power supply variations of $\pm$ 1 %, the maximum comparison rate, for which the comparator still delivered faultless results was measured. The minimum interval between two consecutive comparisons is given by the sum of the maximum comparison time and the time needed for the detection of the comparison result. The number of the "X > A" results per scaler cycle is given by the programmed word.

The threshold of the discriminator for the detection of the "X > A" results (Fig. 12) was set at 80 % of the "X > A" level. This allowed the detection of the amplitude loss of the critical "X > A" comparison results, due to a too rapid sequence of comparisons.

The minimum interval between two comparisons, within the faultless operation range, was measured with 1,9 µs for the transistor comparator and 100 ns for the tunneldiode solution. It was practically independent on the above indicated temperature and power supply variations. The transition from the faultless into the faulty operation region was sharp, in the order of one or several percents of the maximum comparison rate for the transistor or the tunneldiode comparator, respectively. The measuring accuracy was 10^{-6}.

4. Conclusions

The identical lay-out of all stages for the realized comparators, allowing their application as flexible units in a building block system, has been proven as a very useful feature.

For data processing applications, where mostly digital thresholds are needed, two-state comparators are to be prefered to three-state comparators. A two-state comparison can be characterized as a more fundamental logic operation and therefore two-state comparators are in general more flexible in application and in addition simpler in lay-out. For three-state comparisons an adequate combination of two two-state comparators can be used without appreciable additional element needs. Three-state comparators are necessary for regulation purposes, as for instance the stabilization of gain by using digital references .

The realized two-state comparator uses slow tunneldiodes as threshold elements. Faster tunneldiodes would allow an increase in operation speed up to an order of magnitude, if necessary.

A disadvantage of the tunneldiodes as main comparator

elements is their bistable character. Short undesired signal transients, like the undershoot of the reset signal, have to be kept small.

If great operation speed is not needed, a transistor can be used as threshold element also for a two-state comparator. The circuit lay-out of one stage and the quantitative design considerations are given in Fig. 13 and Fig. 14, respectively.

Acknowledgements

Grateful acknowledgements are due to Mr. H. Meyer and Mr. B. Idzerda for their valuable suggestions and comments as well as for their current help during the work, and to Mr. W. Stüber for his stimulating ideas concerning the two-state comparator. Thanks are also due to Mr. R. Vangoidsenhoven for his assistance in realizing the circuits and performing the measurements.

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(7) W. Stüber, Euratom, C.B.N.M. Geel, Private communications.

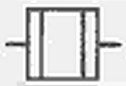
AND

INVERTER

EMITTER FOLLOWER

FLIP-FLOP BINARY

AMPLIFIER



DIGITAL DELAY

TWO STATE COMPARATOR STAGE

THREE STATE COMPARATOR STAGE

DISCRIMINATOR

SCALER

LIST OF CIRCUIT SYMBOLS

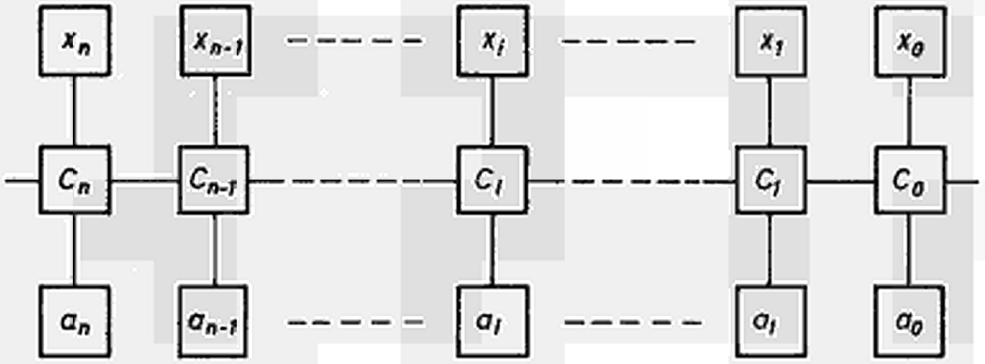


Fig.1 Realized comparator, simplified blockdiagram.

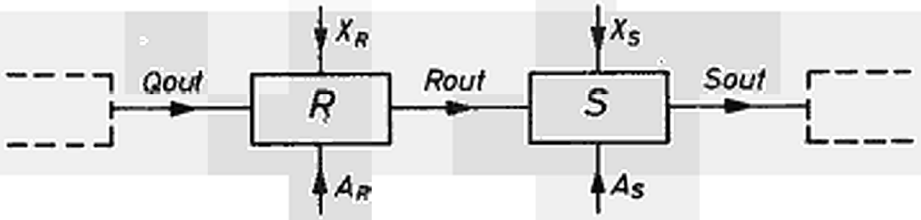


Fig.2 Two cascaded comparator stages.

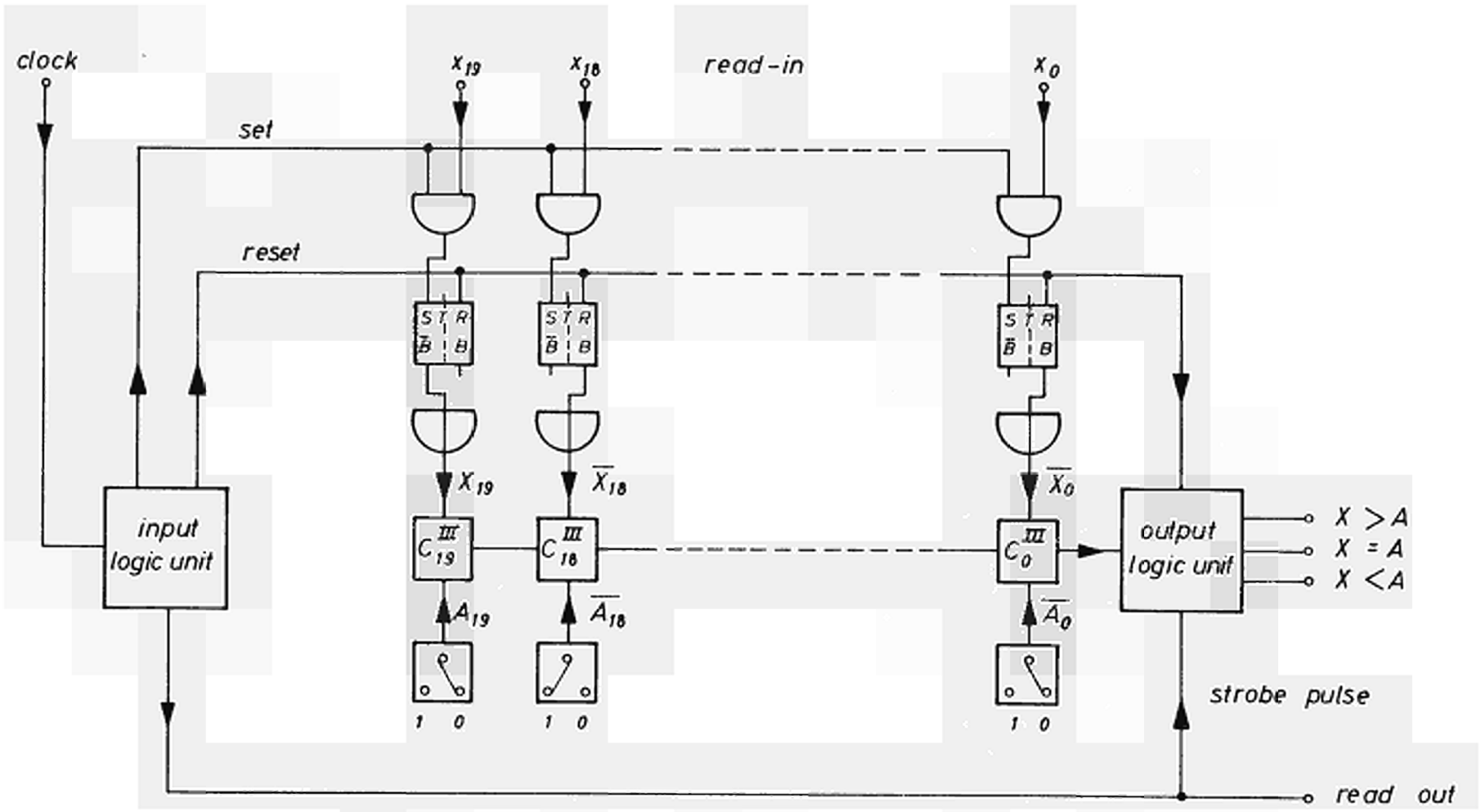
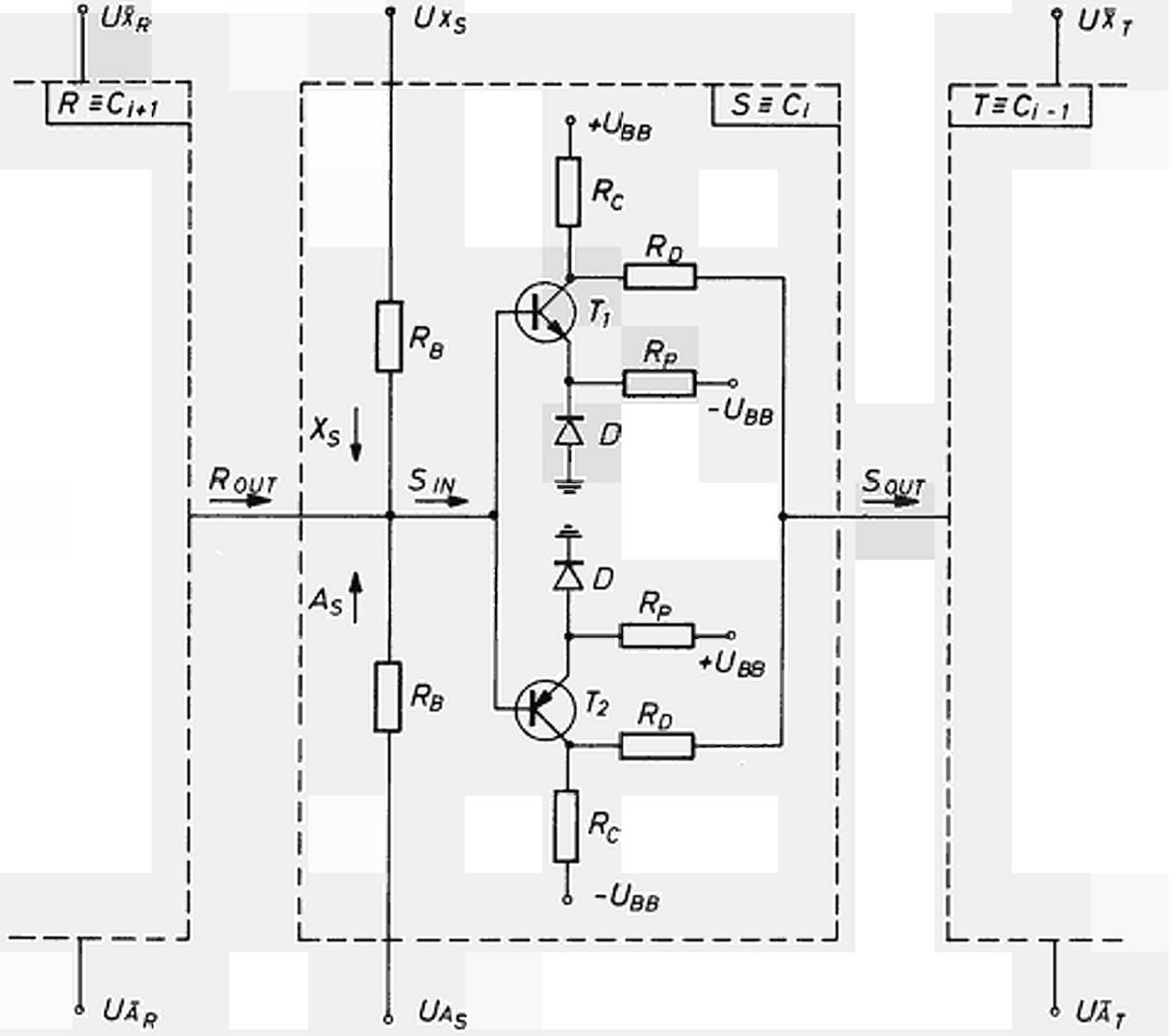


Fig.3 Three-state comparator with transistors, blockdiagram .



$R_P = R_C = 680\,\Omega$; $R_B = 1K8$; $R_D = 390\,\Omega$; $T_1 \equiv 2N708$; $T_2 \equiv FW4138$; $D \equiv 0A85$.

x = "1", $U_X = +4.3\,V$ $\quad$ a = "1", $U_A = -4.3\,V$

x = "0", $U_X = 0\,V$ $\quad$ a = "0", $U_A = 0\,V$

Fig. 4 Three-state transistor comparator, one comparator stage.

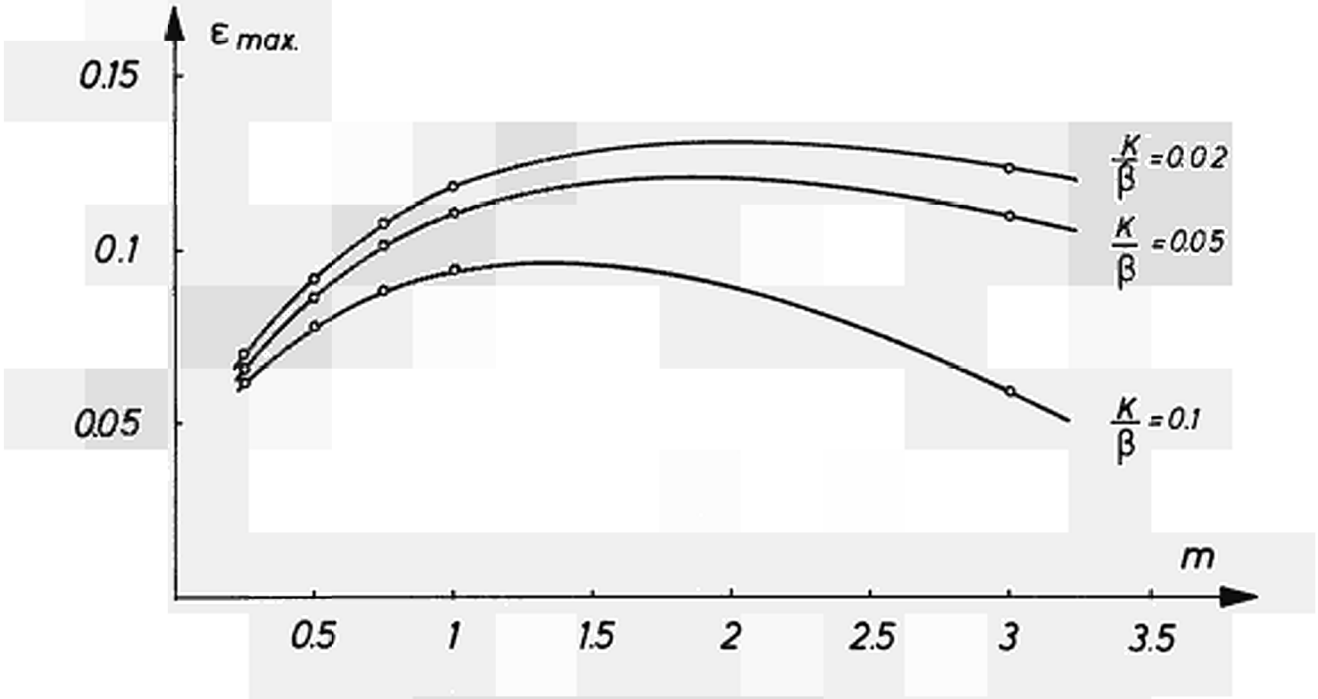


Fig. 5 Three-state transistor comparator in M.L. mode, ε_{max} vs. m for $K_1 = K_2 = K$.

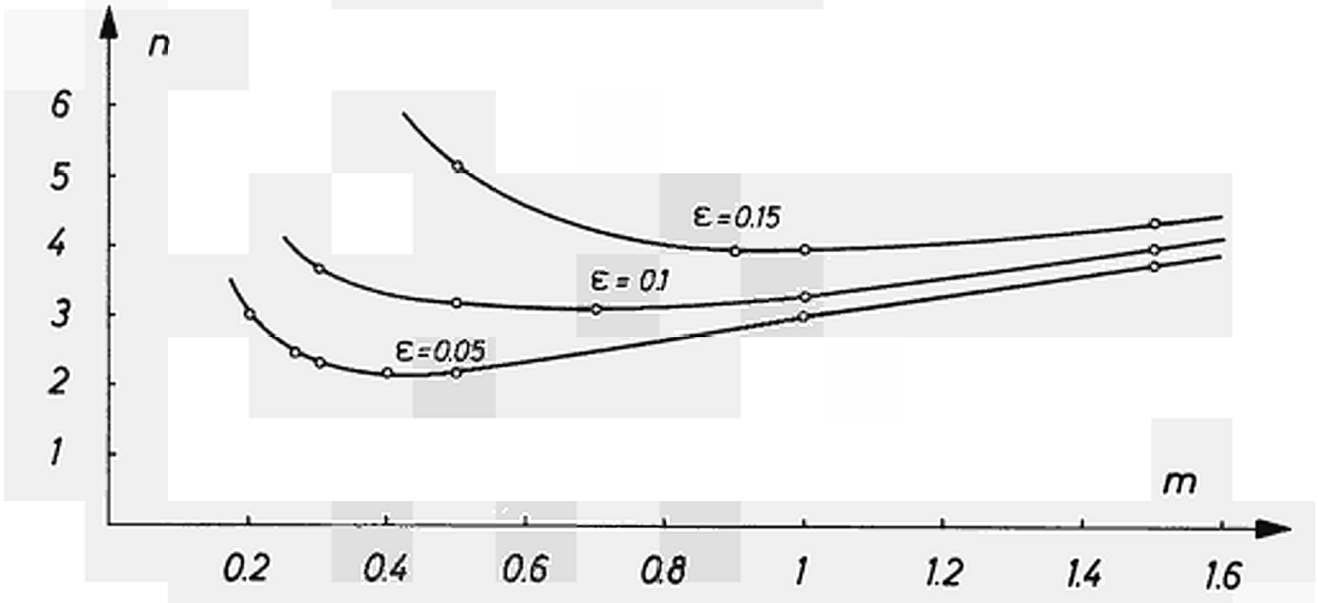


Fig. 6 Three-state transistor comparator in M.L. mode, m vs. n for $K_1 = K_2$.

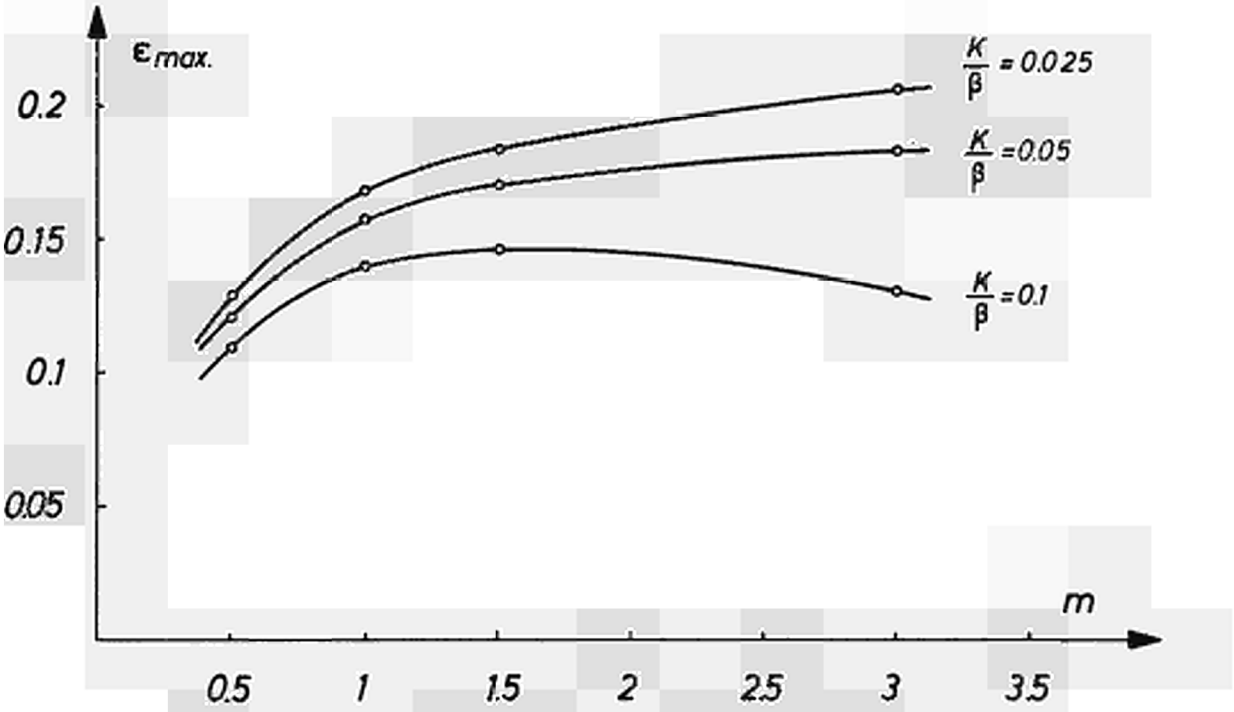


Fig. 7 Three – state transistor comparator in L.M. mode, ϵ_{max} vs. m for $K_1 = K_2 = K$.

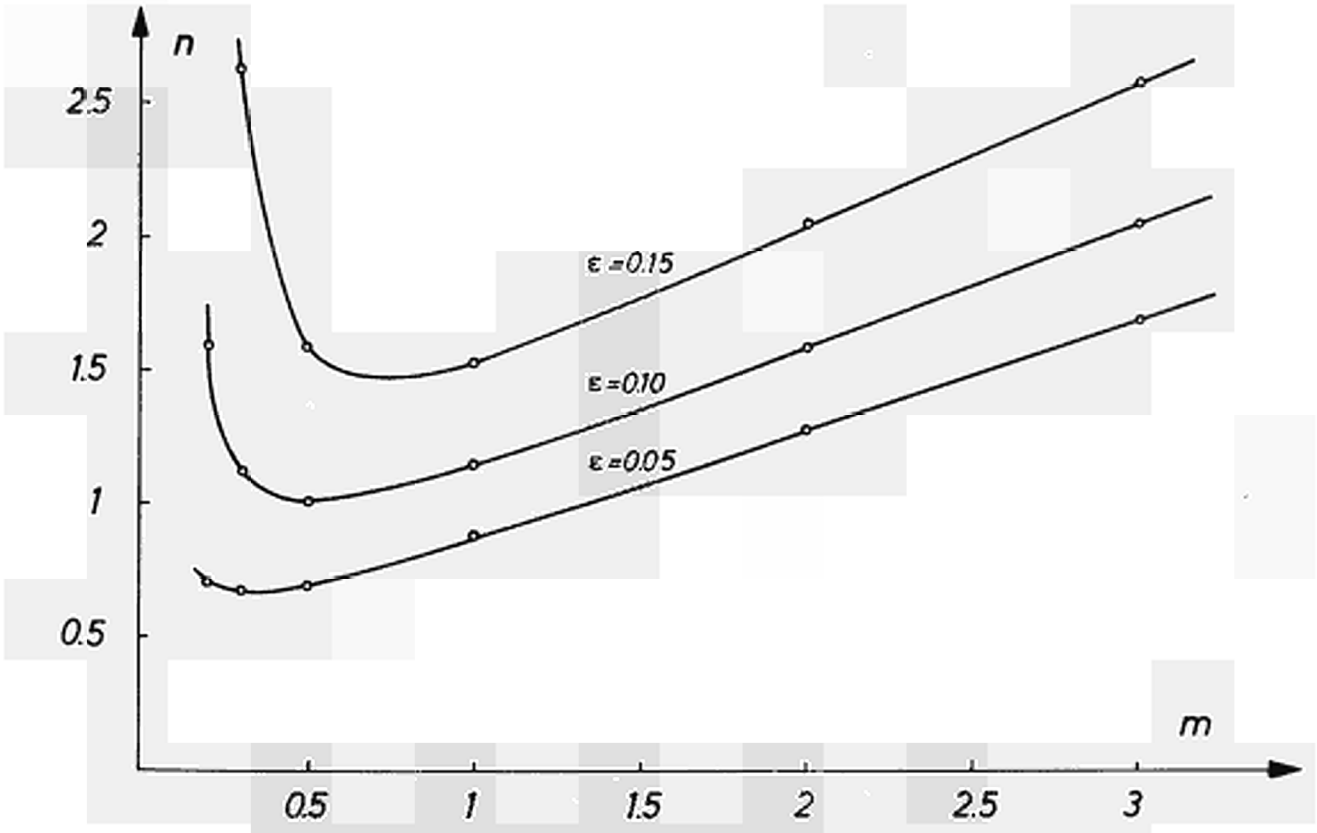


Fig. 8 Three – state transistor comparator in L.M. mode m vs. n for $K_1 = K_2$.

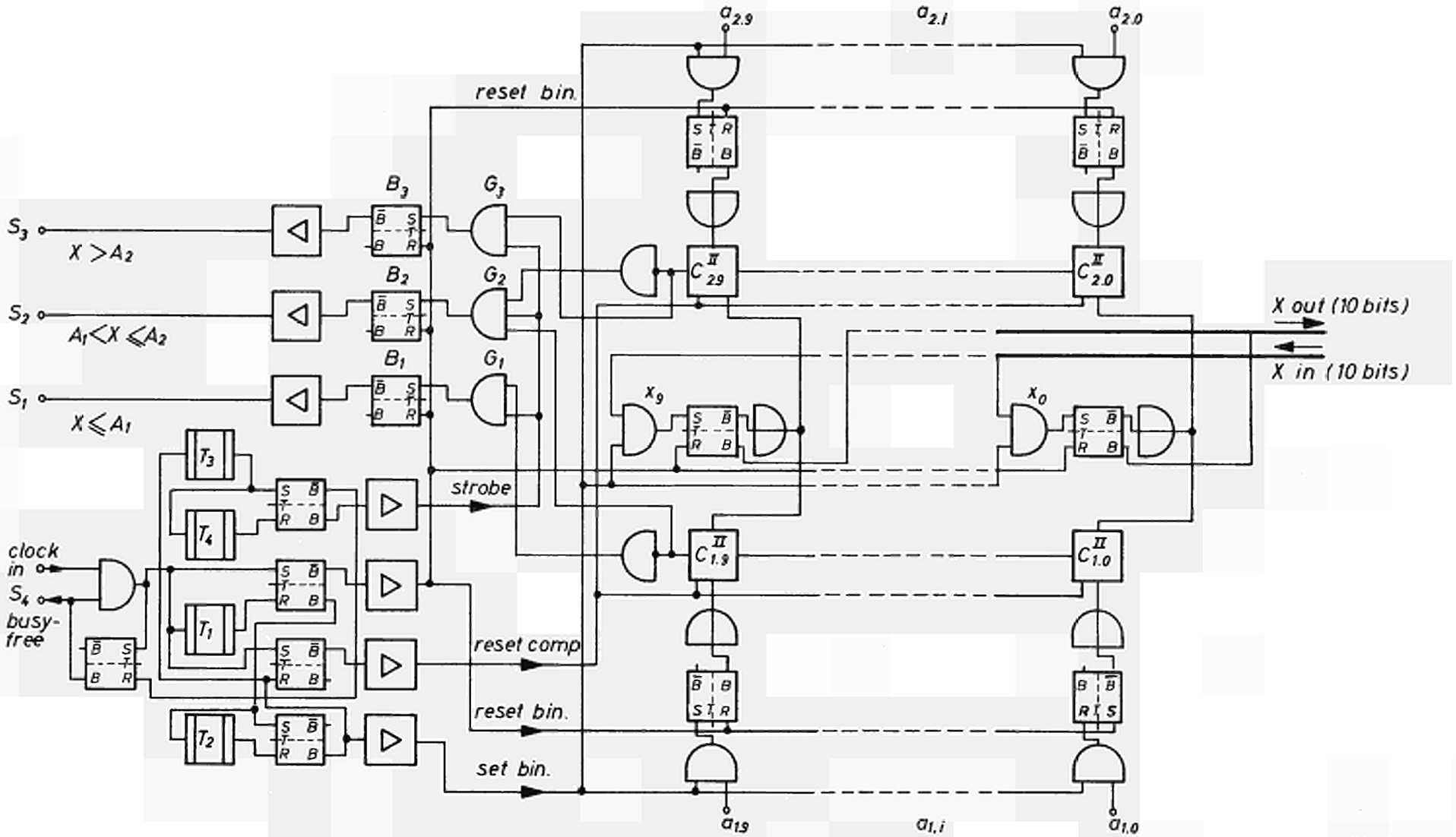


Fig. 9 General block diagram of the window comparator.

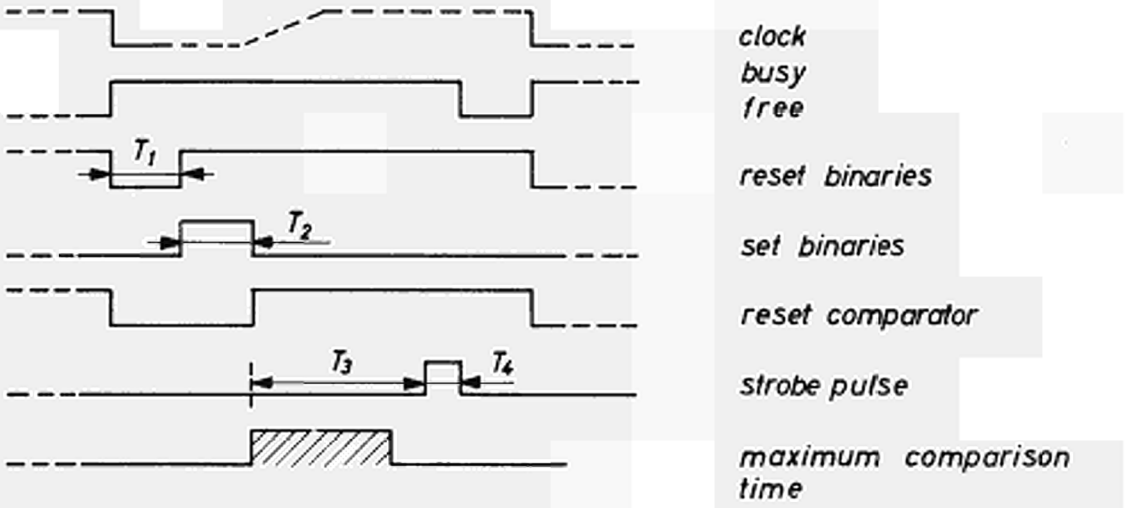
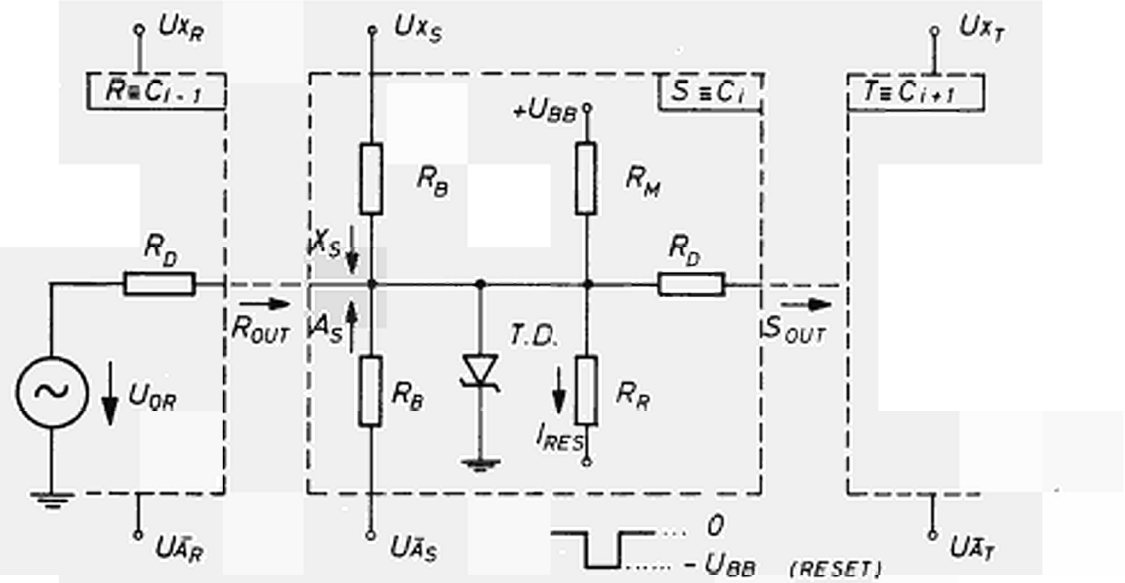


Fig.10 The time diagram of the window comparator.



$R_M = 3K9$; $R_B = 1K8$; $R_D = 150\Omega$

x = "1" , $U_x = +4.3V$; x = "0" , $U_x = 0V$

a = "1" , $U_{\bar{A}} = 0V$; a = "0" , $U_{\bar{A}} = +4.3V$

TD ≙ AEY 11

Fig. 11 Two-state tunneldiode comparator, one comparator stage.

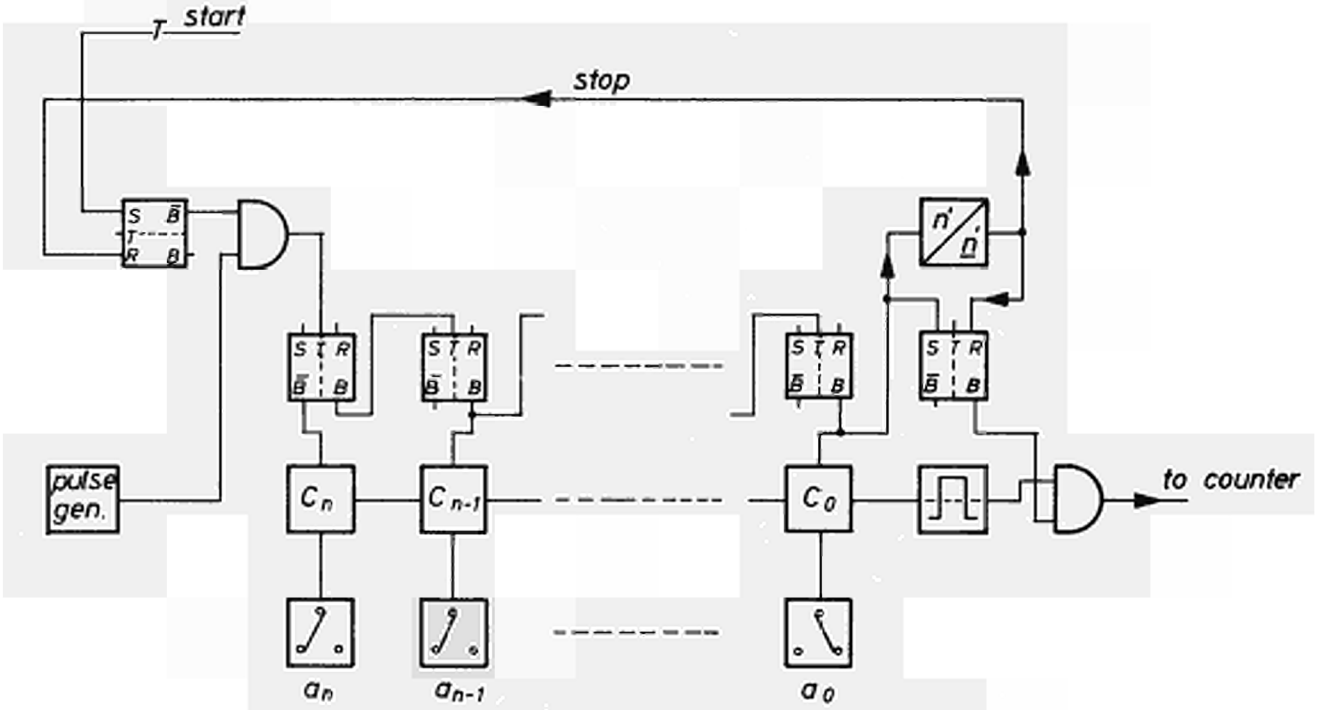
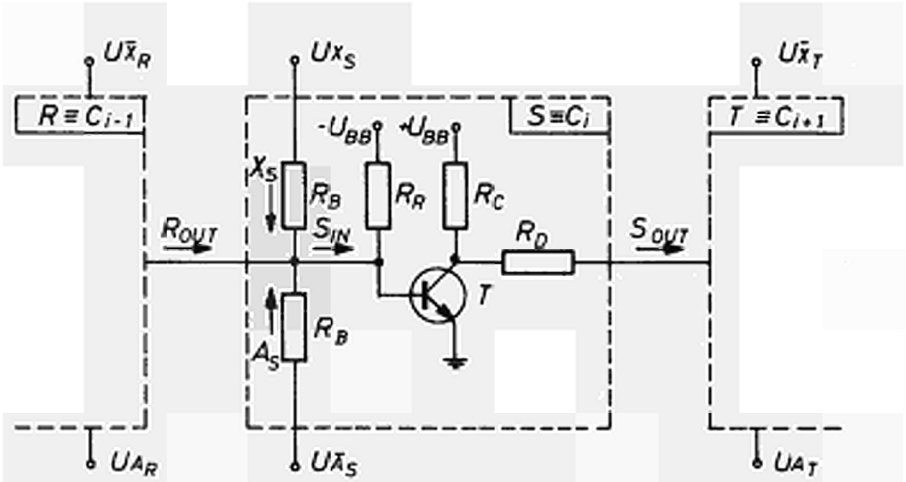


Fig.12 Integral operation test ; blockdiagram.



$$\frac{R_B}{R_C} = n\,; \qquad \frac{R_D}{R_C} = m = \frac{n}{\delta} - 1\,; \qquad \frac{R_R}{R_C} = \frac{1}{\frac{\delta}{n} + \frac{\varepsilon \cdot \delta}{3(n-\delta)}}$$

$x = "1"$, $U_x = +4.3\,V$; $x = "0"$, $U_x = 0$

$a = "1"$, $U_{\bar{A}} = 0\,V$, $a = "0"$, $U_{\bar{A}} = +4.3\,V$

Fig. 13 Two-state transistor comparator, one comparator stage.

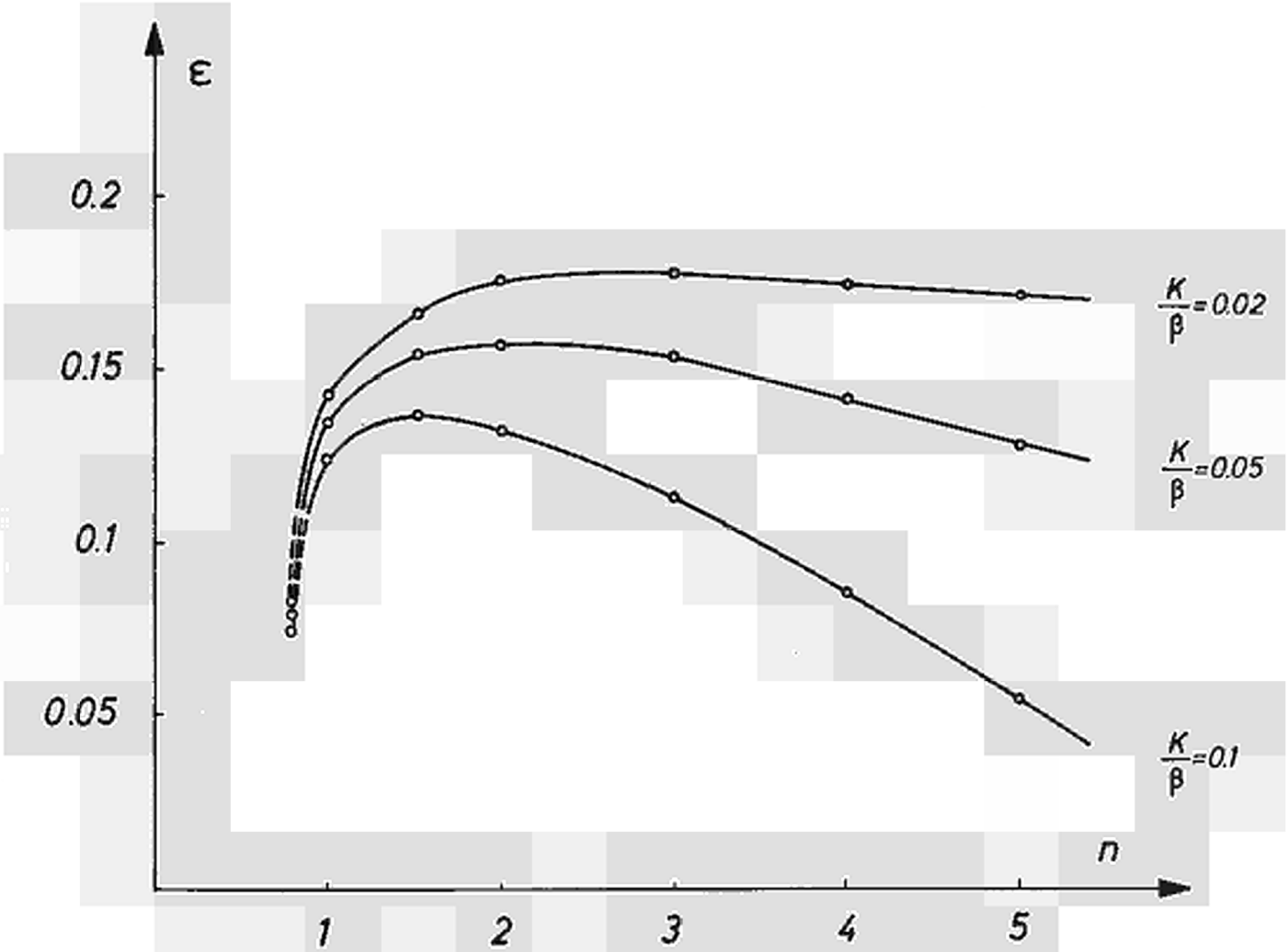


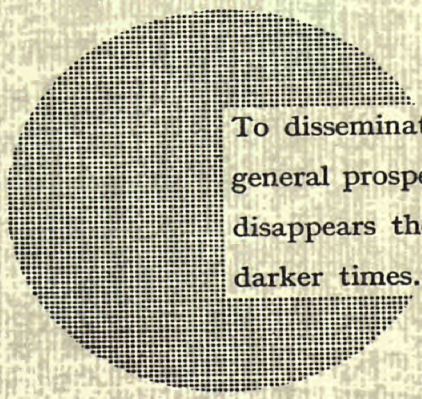
Fig.14 Two-state comparator with transistor, $\varepsilon_{max.}$ vs n.

COMPARISON RESULT OF STAGE "R" AND PRECEDING STAGES	R_{OUT}	X_S	A_S	S_{IN}	S_{OUT}	COMPARISON RESULT OF STAGE "S" AND PRECEDING STAGES
$X = A$	0	0	0	0	0	$X = A$
	0	0	-1	-1	+1	$X < A$
	0	+1	0	+1	-1	$X > A$
	0	+1	-1	0	0	$X = A$
$X > A$	+1	0	0	+Z	-1	$X > A$
	+1	0	-1	+Z-1	-1	
	+1	+1	0	+Z+1	-1	
	+1	+1	-1	+Z	-1	
$X < A$	-1	0	0	-Z	+1	$X < A$
	-1	0	-1	-Z-1	+1	
	-1	+1	0	-Z+1	+1	
	-1	+1	-1	-Z	+1	

Table I *Three–state comparator in M.L. mode .*
Possible comparison conditions of the stage "S".

COMPARISON RESULT OF STAGE "R" AND PRECEDING STAGES	R_{OUT}	X_S	A_S	$\bar{A}_S$	S_{UM}	S_{OUT} (CARRY)	COMPARISON RESULT OF STAGE "S" AND PRECEDING STAGES
$X \leqslant A$	0	0	0	1	1	0	$X \leqslant A$
	0	0	1	0	0	0	$X \leqslant A$
	0	1	0	1	0	1	$X > A$
	0	1	1	0	1	0	$X \leqslant A$
$X > A$	1	0	0	1	0	1	$X > A$
	1	0	1	0	1	0	$X \leqslant A$
	1	1	0	1	1	1	$X > A$
	1	1	1	0	0	1	$X > A$

Table II *Two–state comparator in L.M. mode .*
Possible comparison conditions of the stage "S".



To disseminate knowledge is to disseminate prosperity — I mean general prosperity and not individual riches — and with prosperity disappears the greater part of the evil which is our heritage from darker times.

Alfred Nobel

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