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EUROPEAN ATOMIC ENERGY COMMUNITY - EURATOM

THE EURATOM COMPUTER LINKAGE SYSTEM

by

C. GREEN

1963

Joint Nuclear Research Center
Ispra Establishment — Italy Scientific Data Processing Center — CETIS
(CETIS - Report No 40)

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SUMMARY

This report describes a project for the construction of a system for the linkage of digital and analogue computers. It proposes two principles hitherto unused in this field, namely an asynchronous system for the regulation of the passage of data from the analogue computer to the A-D converters, and an interpolation system at the output of the digital computer. The philosophy of linkage construction is considered and the reasons behind the choice of this method are made explicit. The consequences in terms of hardware are examined at length and finally the future prospects of the scheme are estimated.

1 — PREVIOUS WORK IN THE FIELD

Analogue-digital linkages have been in existence for several years and have already been applied successfully to some classes of problems. The devices at present available commercially however have certain disadvantages closely related to their origins, since they were mostly developed for either digital reduction of analogue trials data, particularly in the aircraft industry, or for hybrid control systems, for example for nuclear power generators. In these fields the requirements for accuracy are not so stringent as in a computation centre, and since these are « special purpose » systems the control of the conversion can be very simple. Nevertheless the accuracy and speed of converters have been extensively studied in recent years and the Euratom request for quotations for a converter system revealed the existence of a number of fast, accurate, converters. At the same time these quotations demonstrated that the control needs of a linkage system suitable for computation centre use have not yet received study commensurate with that devoted to the converters themselves and thus there exists at present no genuine general purpose linkage. In addition the staircase type output from the D-A converters, which is used in all present day machines, is quite unacceptable for accurate work, as shown by the following simple calculations : Take a sinusoidal function for D-A conversion with a frequency of 1 cycle/sec. Referring amplitudes to the analogue computer scale of ± 100 volts, the maximum gradient of the sine wave is 200 volts/sec. Assuming a system data rate of 10 KC at the A-D converter the no. of points per sec. per channel at the D-A side will be 500 for a 20 channel system.

The variation between steps of the staircase will thus reach $\frac{200}{500}\pi$ volts or more than 1.2 volts which implies errors reaching 1 % of full scale for a frequency of only 1 cycle per second. As a result of this it is considered that the Euratom system must incorporate linear interpolation in the D-A conversion (there seems to be no advantage in higher order interpolation).

To return to the control of the linkage, with only one exception the systems offered to us depended entirely on a rigid clock control. Now this is highly undesirable from the standpoint of accuracy since the available data rate is held at its lower limit regardless of wide differences between the requirements of the channels and their continual change through time. Even more disastrous is the economic effect of a synchronised system. A 10 K/C A-D converter can virtually saturate the IBM 7090 computer and in a synchronised system this saturation remains as long as running continues, whereas the number of transfers necessary in a selective,

asynchronous, system would probably not exceed one fifth of maximum and would have an effective response 5 times faster. Thus if in the economics of the system one includes running cost as well as purchase price, it proves worthwhile to invest a substantial sum in the development of a selective control system.

2 — GENERAL FEATURES GOVERNING THE DESIGN OF THE EURATOM LINKAGE

The principles adopted for the project design are these :

— The best accuracy available with existing techniques, this implies the use of interpolation at the D-A converter.

— The most economical use of data transmission, ensuring the best operating economy in the use of the 7090 and also maximum accuracy, since the system will continuously adjust the data rate of the channels according to the incoming signals.

— The integration of the system into the framework provided by the general automation project for the analogue computer, involving the APACHE ([1]) coding programme and making provision for the automatically set up patch panel which could be built into the system. An important facility to be included is that for plotting digital results under complete 7090 control.

— The best use of the possibilities of the 7090 system.

This feature was notably, if understandably, lacking in the all quotations received here.

It would not be very helpful to present to manufacturers these principles without some ideas on realisation possibilities and accordingly the following project design has been drawn up. It is to be emphasized that this account is to be taken as a guide rather than as a specification. If engineering experience suggests other methods of procedure, we of Euratom will be pleased to hear of them. The account has been prepared by programmers of analogue and digital machines, and, although we have taken engineering advice wherever possible, it is expected that the general organisation and the functional design will stand up to scrutiny better than the suggestions for construction of the equipment.

Granted this disclaimer, however, it is felt that the proposals are extremely promising, and contacts with constructors have uniformly tended to reinforce this notion.

3 — DESCRIPTION OF THE LINKAGE SYSTEM PROJECTED

Flexibility is maintained throughout by the principle that each stage of data transfer should be proceed at its own speed and call into action the next stage when its own part is complete.

Thus the A-D conversion will take place when the analogue input has changed sufficiently to render it necessary. Thereupon, the conversion being complete, the digital computer will be called into action, and will itself call the D-A conversion into operation when the processing is complete.

([1]) A description of the APACHE system will be found in the abstracts of the 3rd International Conference on Analogue Computing ; it is felt that the engineers studying the described analogue to digital linkage should be familiar with the APACHE ; pre-prints of this paper are available from Euratom.

3.1 — The analogue to digital control

Referring to the diagram, the system will be traced through this operating loop. The analogue variables are patched to a « Track and Hold Gate » and may also be connected to a « Control Trigger », which has previously been set up by the digital machine. If one of these analogue signals touches either of its limits the Control Trigger will fire, signalling both the « Linkage Addressing Matrix » (LAM) and the « Priority Delay Line » (PDL). The LAM is a matrix up to 20 × 20 in size, set up by programme before the problem is run, which relates each incoming signal to a group of from 1 to 20 outputs.

The Trigger signal thus arrives at a group of Track and Hold Gates which freeze the appropriate channels. Let us note that the number of control triggers could be 20 but in general a smaller number will suffice.

The PDL has a cycle depending on the time for multiplexing and converting one signal, and at the beginning of each cycle selects the signal of highest priority according to the numerical order of the triggers. A signal once selected retains top priority as long as the « repeater signal » lasts (1).

When a channel signal is passed out of the PDL, it goes through the same path in the LAM as the corresponding trigger signal but because of its different form affects only the « Second Priority Line » (SPL) and not the Track and Hold Gates. When the SPL receives a single channel signal it is transmitted in this channel to the AD Multiplexer which the routes the same channel to the A-D Converter. If two or more channels arrive simultaneously then only the first will be passed and will then be inhibited at the next passage. The « Repeater » signal will then be turned on and will cause the PDL to repeat the same channel until there is only one signal left. At this stage all inhibiters are cancelled and the next group can be accepted. Thus the PDL determines the priority of the group and the SPL priority within a group.

Data passed to the converter will be immediately converted and passed in serial form into the A-D buffer. The address to which it is to be sent in 7090 memory is taken from a fixed table of up to 20 addresses, each of 15 bits.

These addresses have no significance for the linkage programme, and thus must not be programme set. It might be possible to retain a certain group of addresses in absolutely permanent form, but this is undesirable from the point of view of production planning since the linkage programme must be compatible with the largest possible range of digital programmes which may thus be run simultaneously.

Accordingly it is proposed to set the first 10 digits of the address group by a set of manual switches and to have the last five digits permanently wired to give the numbers from 0 to 19.

When the PDL has passed a sufficient part of its cycle to permit the A-D buffer to be filled it sends a « B cycle » demand to the multiplexer of the 7090 which will be accepted (and cancelled) when the multiplexer is ready (about 1 microsecond) causing the multiplexer to interrogate the selected address and the data register and to store the data in the appropriate memory position.

Until the « B cycle » answers, the PDL passes no more conversion signals. Whenever a « Repeater signal » is received a signal is passed at the end of the cycle to the Input Address Stepper (IAS) thus causing the data of one group to be stored in successive 7090 locations. If there is no repeater signal the IAS is reset and an « Interrupt » signal sent to the Central Processing Unit (CPU) of the 7090. This Interrupt is a continuous signal which remains until

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(1) The PDL cycle ceases if no triggers are on and recommences immediately at the next signal.

the operation in progress is complete (a few microseconds). When it is accepted control is passed to the instruction indicated by the interrupt address which is simultaneously transferred to the Interrupt Address Buffer enabling immediate entry into the appropriate processing programming. There are two interlocks here which can stop the PDL, the first on the non-acceptance of the « Interrupt » and the second on the non-appearance of the « Input Memory Clear » (IMC) signal furnished by the programme as soon as the data from the input memories has been transferred.

There remain a few additional features on the A-D side.

The first is the existence of a group of about 10 « Functional Control Triggers » which can generate Interrupt signals for programmes requiring no input from the analogue machine. These Triggers will be required for such functions as plotting of digital data. Secondly it is desirable to have at each of the 20 inputs a multiposition mechanical switch set or stepped by programme enabling the automatic selection of variables for conversion in static functioning. One could take 8 or 10 positions per channel according to the type of switch proposed.

Thirdly for functions of the transport delay type an additional integrater is required before the control voltage can be fed to the control triggers, since the rate of transport is the function appearing as a problem variable. This integrator will feed the control trigger directly and for this application the control trigger limits will be symmetric and pre-set. The transport rate must be made available with both signs and the input to the integrater will be switched whenever the control trigger fires.

Fourthly for certain functions the control of an accurate clock is necessary, e. g. in iterative calculations. It is proposed to incorporate the clock directly into the PDL by-passing the triggers.

3.2 — The Digital to Analogue Control

When the 7090 has completed its processing it stocks the data to be output in a set of consecutive locations determined by manual setting up as in the case of the input. These will be selected in rotation by the Output Address Stepper, which functions in almost the same manner as the « IAS ». This implies that if overwriting is to be avoided the Output Memory Clear signal must be sent to the PDL before a new Interrupt can be admitted and thus that the time required by the output device to clear these memories must be added to the digital processing time in calculating the effective data rate. This can be avoided if a double set of output stores be used. Each digital programme must then appeal to a common subroutine and the OAS must be a circular device with 2 reset points. This will not be necessary if the output can be made fast enough, but present estimations are that the output time will be much too long to permit the simpler system.

The actual form of the output words will not be known until the detailed design of the D-A Multiplexer is undertaken since these two items are interdependent, however the overall process is clear. At the end of the processing programme a signal of the same type as that used for calling the 7090 channels into operation is sent from the CPU to the Linkage Output Control (LOC). The 7090 will pass to its next job immediately after this signal is sent and if the LOC is not ready it remembers the signal and obeys it as soon as it is free. This system keeps free the most expensive unit for the maximum time. The LOC then sends a « B-cycle » demand to the 7090 Multiplexer which when ready permits the passage of information from the address shown on the OAS to the output buffer. In the output buffer it is examined for the presence of the « continuation bit » signifying that the transmission of a group of outputs is not yet completed. If the continuation bit is present the LOC will send another B-cycle as soon as it is free and will also cause the OAS to step. If there is no bit the OAS will advance to reset

position. Information in the first output buffer will be immediately passed to the D-A Fast Multiplexer which will route it to the appropriate converter buffer or to the Slow Multiplexer buffer. The address is to be transferred as part of the data. As soon as the data is established in the appropriate buffer the LOC is released, probably by a time delay in the case of data which does not pass through the Slow Multiplexer, but otherwise by a signal. Data reaching the D-A converter buffers will be converted to analogue form by the interpolating converters (see next section) the « Convert » signal being contained in the data transmitted by the Fast Multiplexer. The Slow Multiplexer will be used to fulfill all the static set up functions of the linkage and in most cases the units in question will in fact act as buffers.

These static linkage units will include

— the Linkage Addrcssing Matrix and D-A converter modes,
— Linkage input and output selectors,
— the ADIOS system, data and controls,
— the Analogue machine modes and other controls for several machines,
— a group of digital potentiometers (relays switching in standard resisters),
— the eventual automatic patching system,
— a group of relays for logical control of the analogue consoles (not with automatic patching)
— dataplotter controls.

In every case the unit in question will signal the LOC when the data has been read. This will enable the 7090 to pass set up information in batches which will be interpreted at the rhythm of the receiving device. To call the 7090 at the end of an information group a « Recall bit » must be provided which causes the LOC to fire a Functional Trigger.

The control interlocks on the D-A side are the Output Memory Clear, sent from the LOC and the clearing of the « B-cycle » and also the final buffer clear signals. In addition to this both A-D and D-A sides should interlock with the hold of the analogue machine for dynamic functioning though not for transfers to the static set up buffers. For completeness the same type of programme controlled selector could be used at D-A output as at A-D input.

3.3 — **Interpolating D-A converters**

These devices function according to the relation

$$Y = Y1 + W1\,(X - X1)$$

where X1, Y1 is a point of the line of which the segment chosen represents the curve in a given region and W1 is its slope at that point. Note that X1, Y1 is not necessarily a point of the curve. The region of validity must then be defined by two limits, in general X2, X3 (See figure 2).

Note first that the generality of this representation, which might seem excessive at first glance, can be used to facilitate the construction in such a way as to render the total assembly more simple. The layout of the generalised converter is shown in figure 3. Here the point of vital importance is that only the Y1 must be converted with the full number of bits for maximum accuracy, since thc W1 (X-X1) term can be maintained as a small correction term, and the accuracy requirements on the limits are notably less severe than on Y1.

It is for this reason that the above formula is not to be simplified as

$$Y = Y1 - W1 \times X1 + W1 \times X$$

which would give the multiplicative term the same importance as the constant. The next point to note is the generation of the product term. As shown in the diagram all the other converters are fed directly by the analogue computor reference, but in this case a problem

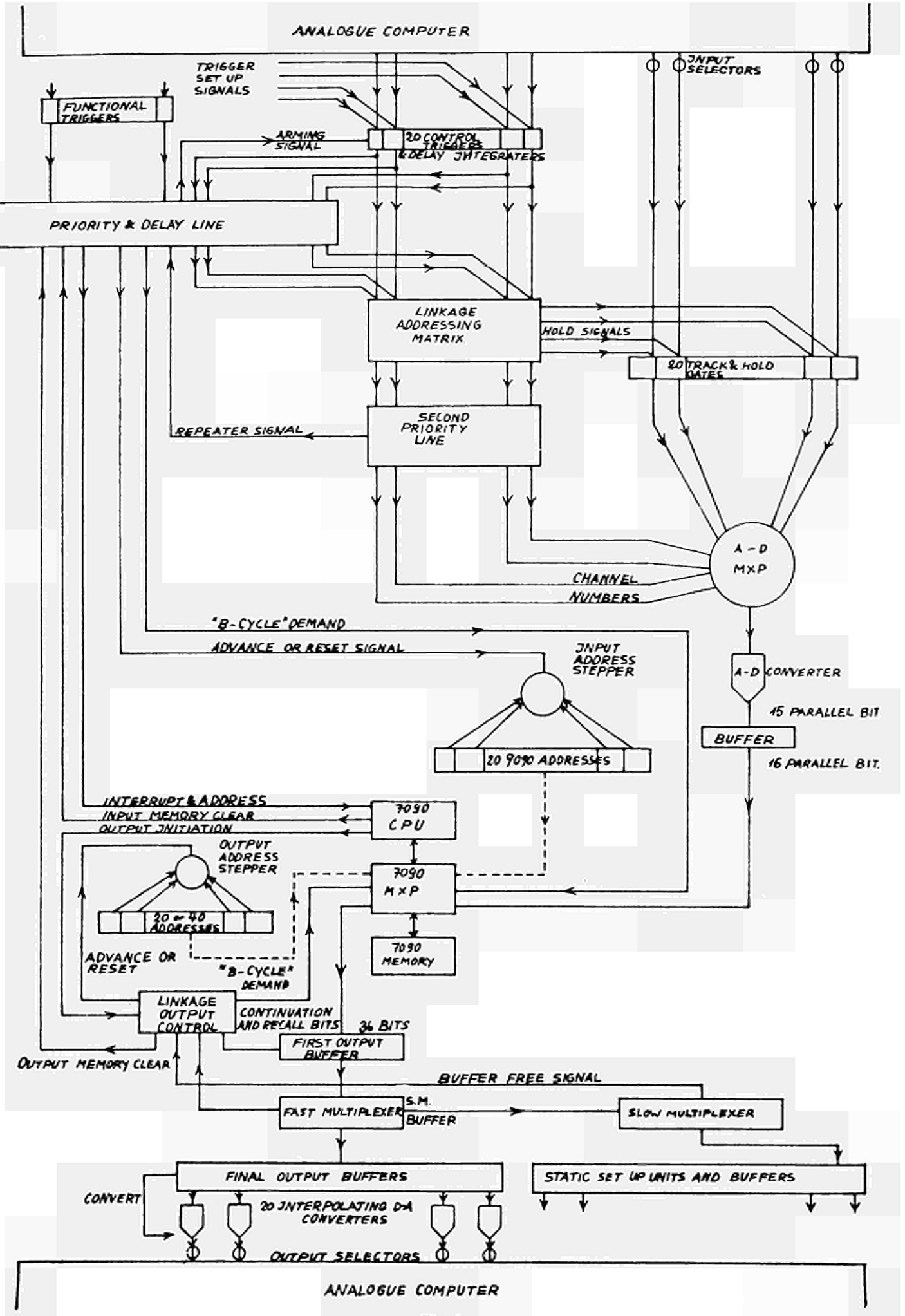
ANALOGUE COMPUTER
TRIGGER SET UP SIGNALS
INPUT SELECTORS
FUNCTIONAL TRIGGERS
ARMING SIGNAL
20 CONTROL TRIGGERS & DELAY INTEGRATORS
PRIORITY & DELAY LINE
LINKAGE ADDRESSING MATRIX
HOLD SIGNALS
20 TRACK & HOLD GATES
SECOND PRIORITY LINE
REPEATER SIGNAL
A - D MXP
CHANNEL NUMBERS
"B-CYCLE" DEMAND
ADVANCE OR RESET SIGNAL
INPUT ADDRESS STEPPER
A-D CONVERTER
15 PARALLEL BIT
BUFFER
16 PARALLEL BIT
20 9090 ADDRESSES
INTERRUPT & ADDRESS
INPUT MEMORY CLEAR
OUTPUT INITIATION
7090 CPU
OUTPUT ADDRESS STEPPER
7090 MXP
20 or 40 ADDRESSES
7090 MEMORY
ADVANCE OR RESET
"B-CYCLE" DEMAND
LINKAGE OUTPUT CONTROL
CONTINUATION AND RECALL BITS
36 BITS
FIRST OUTPUT BUFFER
OUTPUT MEMORY CLEAR
BUFFER FREE SIGNAL
FAST MULTIPLEXER
S.M. BUFFER
SLOW MULTIPLEXER
FINAL OUTPUT BUFFERS
STATIC SET UP UNITS AND BUFFERS
CONVERT
20 INTERPOLATING D/A CONVERTERS
OUTPUT SELECTORS
ANALOGUE COMPUTER

Fig. 1.

Fig. 2.

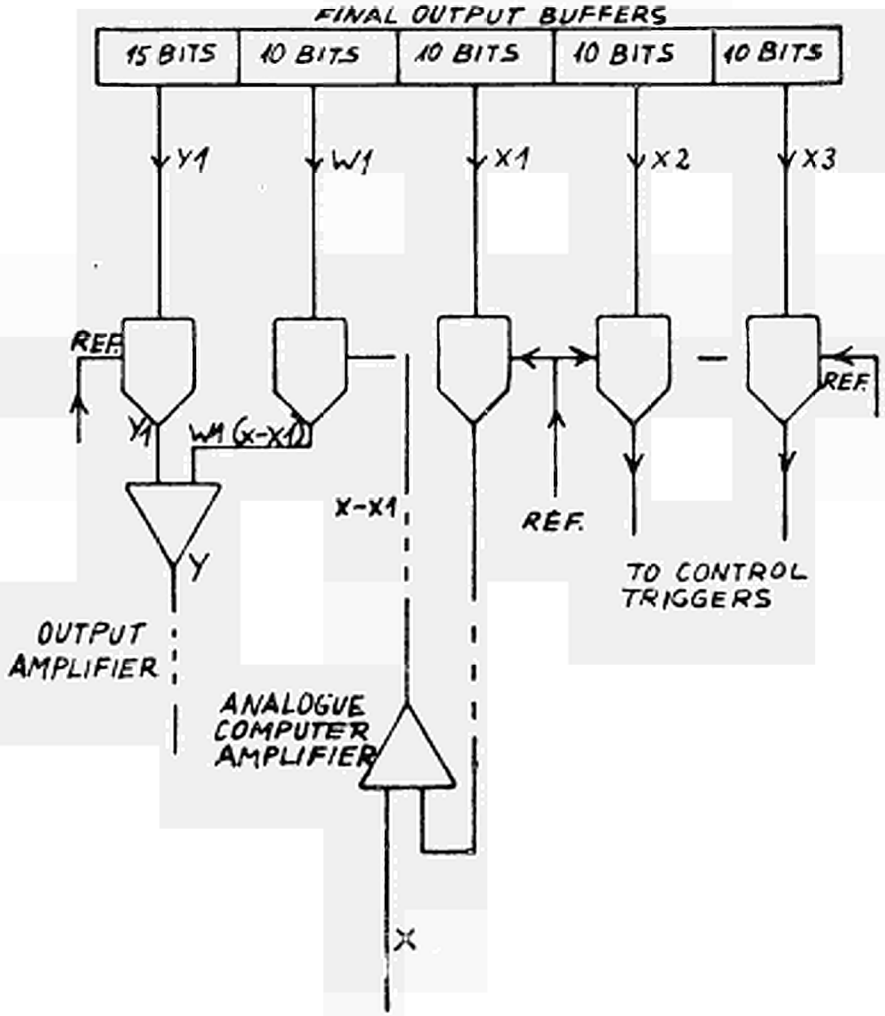

Fig. 3.

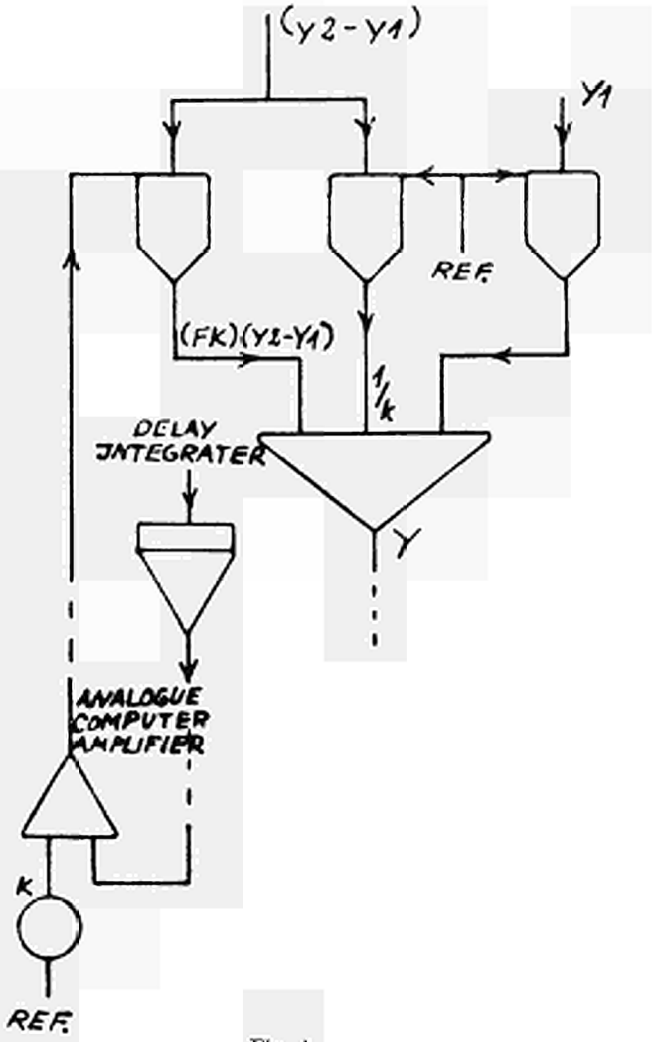

Fig. 4.

variable replaces the reference. Since the solid state elements are highly non-linear this is not likely to be acceptable in the general case, at any rate according to our experiment with diode gates in Ispra, although we would be happy to have news to the contrary. On the other hand the same experiment suggested that if the range of X — X1 is limited to one sign and excludes the region around zero the required accuracy could be obtained. It is for this reason that the notion of making X1 equal to X2 is to be rejected. Next the idea of using only a limited set of D-A converters with a multiplexing to a set of memories at the analogue side. Failing contrary experience the problem of setting up analogue memories sufficiently rapidly seems difficult to solve since the converters must supply the final multiplexer at least 10 KC/S. Thus the solution of one 15-bit and four 10-bit D-A converters per channel is the one preferred here. A useful point to note is that for functioning in the time delay mode of operation calculation can be saved by taking the (X — X1) term direct from the delay integrater. The interpolation can be expressed in this case by the equation

$$Y = Y1 + K\,(Y2 - Y1) + (T - K)\,(Y2 - Y1)$$

where T is the output of the delay integrater and K is a constant. The connection for this case is shown in figure 4 and indicates that one converter is still available to shift the origin of the multiplicative term. To note also is the provision of a range of scale factors (binary powers) for the W1 term.

4 — CONCLUSIONS

This report is intended to define the principles of the Euratom linkage and to try to indicate a path towards its' realisation. It is felt that while the needs of Euratom may seem novel, they are nonetheless common to all computation facilities above a certain minimum size. In addition it is considered that *only* by the type of organisation described can a satisfactory *general purpose* linkage system be constructed. The case of handling functions of several variables by this method is notable, but the very great expansion of logical possibilities leading to rapid iteration programmes, automated optimisation, and digital overseeing and processing of the analogue results, render this linkage totally different from its predecessors in the scope of its possibilities. In short it is a step towards the integration of the two types of computer to form a genuine hybrid, rather than a slender coupling. We are, of course, still prepared to debate this view in the context of utilisation of the final product, but we would prefer to sacrifice the number of channels proposed rather than the overall principles. In any case the number of channels is very hard to define without operational experience but in principle it is highly desirable that the final plan should leave room for easy expansion, particularly of the logic units.

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