COMMISSION OF THE EUROPEAN COMMUNITIES

COM(81) 559 final
Brussels, 8 October 1981

Amended Proposal for a
COUNCIL REGULATION (EEC)

concerning Community actions in the field of
microelectronic technology

(submitted to the Council by the Commission
pursuant to the second paragraph of Article
149 of the EEC Treaty)

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AMENDED
PROPOSAL FOR A COUNCIL REGULATION (EEC)
CONCERNING COMMUNITY ACTIONS IN THE FIELD
OF MICROELECTRONIC TECHNOLOGY
(PROPOSAL MODIFIED IN ACCORDANCE WITH ARTICLE 149, 2ND PARAGRAPH
OF THE EEC TREATY

THE COUNCIL OF THE EUROPEAN COMMUNITIES,

Having regard to the Treaty establishing the European Economic Community, and in particular Article 235 thereof,

Having regard to the proposal from the Commission,

Having regard to the Opinion of the European Parliament (1),

Having regard to the Opinion of the Economic and Social Committee (2),

Whereas microelectronic technology is essential to the development and competitiveness of Community industry as a whole, at a time when the European economy must increasingly provide high added value goods and services; whereas, however, the scale and nature of the effort needed to match the effort of competitors by 1985 require a Community approach which must include public financial support for collaborative research and development by industry; whereas the Council Resolution of 11 September 1979 (3) invites the Commission to explore methods of coordinating national policies and to submit to the Council specific projects at Community level with a view to promoting microelectronic technology,

Whereas the aid granted should aim at furthering a balanced market and competition situation in the Community and taking into consideration the principles expressed in Council Regulation (EEC) No 1996/79 of 11 September 1979 on a Community support mechanism in the field of data processing(4), not least the principles of the ownership of and access to results of supported projects, and thereby underlining in particular the importance of an adequate dissemination of goods and results of supported projects,

HAS ADOPTED THIS REGULATION:

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(1)
(2)
(3) OJ N° C 231, 13.09.1979, p. 1
(4) OJ N° L 231, 13.09.1979, p. 1

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ARTICLE 1

In order to attain the Community objectives concerning microelectronic technology, coordination at Community level of the activities undertaken in the Member States in this domain and implementation of joint projects to supplement and reinforce these activities shall be carried out under the conditions set out in this Regulation.

TITLE 1

Information and Consultation

ARTICLE 2

A system for information and consultation concerning initiatives aimed at promoting the diffusion and the development of microelectronic technology and its application is hereby established between the Member States and the Commission.

ARTICLE 3

1. In order to ensure that the consultations provided for in this Regulation are effective, Member States shall, independently of their obligations under the rules of competition, supply the Commission without delay on their own initiative, or at the Commission's request, with sufficient up to date advance information of a scientific, economic and financial nature concerning any activities under their authority both in progress on the date this Regulation enters into force and contemplated after that date, adressed to:

   a) the promotion of industrial research and development on equipment, processes, instruments and techniques, both hardware and software, for use in the design, industrial manufacture and testing of advanced integrated circuits;

   b) the dissemination of basic knowledge and training and education of management and staff specializing in the design, utilization and testing of advanced integrated circuits;

   c) the encouragement of the establishment within the Community of an industry capable of designing and producing the equipment, materials and techniques used in the manufacture of advanced integrated circuits.

   They shall also supply the Commission with an appraisal of the results of all these activities.
   Information concerning projects which are the sole property of a company shall not be covered by this Article.

2. The Commission, in order to coordinate the action of the Member States shall ensure that they receive the information concerning activities referred to in paragraph 1;

3. After consulting the Committee referred to in Article 6, the Commission shall specify the level of detail of the information to be made available by Member States and of that to be given diffusion, as well as procedures and measures for making this information available to Member States.

TITLE II

Joint projects

ARTICLE 4

1. The following key research and development projects, coming directly within the sectors defined in Article 3 and regarded as having highest priority, shall benefit from Community support under the terms laid down in Article 5.

   (I) step and repeat on wafer
   (II) electron beam for direct-writing on wafer
   (III) plasma etching and deposition
   IV) testing equipment
   (V) Computer Aided Design (CAD) for Very Large Scale Integration circuitry (VLSI) in the domains of
      1. Architecture
      2. Language and Data structure
      3. Testing
      4. Device modeling

2. The technical specifications for the projects specified at point 1 above are set out in the annex.

3. The Commission, in consultation with the Committee referred to in Article 6, shall update the technical specifications as may be required.

ARTICLE 4 BIS

When allocating national public support money to projects related to the sectors defined in Article 3, Member States shall give priority, all other conditions being equal, to those whose execution involves a significant participation of organizations from two or more Community countries.

TITLE III

Financing procedures

ARTICLE 5

1. From 1981 the European Community shall provide financial support to the projects specified in article 4 (1) in the form of a grant of up to 50% of the costs of their execution.

2. The appropriations necessary to this end, now evaluated at ECUS Mio 52, shall be entered in the budget of the European Community.

3. Projects eligible for aid shall meet the following conditions:

   - their purpose must be in line with the technical specifications set out in the Annex referred to in Article 4 (2);

   - the projects must be carried out within the Community;

   Furthermore:

   a) for projects I to IV of Article 4(1)

      - the applicants must be manufacturers or industrial users established in the Community;

      - a sufficient number of firms from at least two Community countries not having financial links with the manufacturer or manufacturers taking part in the same project must have provided evidence of their interest in participating in the project and contributing their own resources. This number shall be decided by the Commission, for each project, after consultation of the Committee mentioned in article 6.

   b) for projects falling under V of Article 4(1)

      - the applicants must be universities, research centres of firms established in the Community;

      - a sufficient number of firms from at least two Community countries not having financial links with each other must have provided evidence of their interest in participating in the project and contributing their own resources.
      This number shall be decided by the Commission, after consultation of the Committee mentioned in article 6.

4. Once the eligibility of the project has been established under the terms of paragraph 3.a) or b), all suitably qualified firms established in the Community may take part in the project and apply for the relevant financial support irrespectively of their possible financial links with other participants in the same project.

5. Applications shall be addressed to the Commission by the organisations concerned in response to call for proposals published in the Official Journal of the European Communities. They shall show evidence that they are justified under the terms of paragraph 3 above and shall provide any other relevant informations. The Commission may request any documents and additional informations required for constituting the dossier.

6. The Commission shall act on applications forwarded to it within a period of six months in accordance with the procedure set out in Article 8.

7. Without prejudice to the powers of the Court of Auditors pursuant to article 206 a(3) of the EEC Treaty, the Commission may carry out investigations on the spot or inquiries into the operations financed .

TITLE IV

General provisions

ARTICLE 6

1. A Coordinating Committee, hereinafter called the Committee, is hereby set up to coordinate projects promoting microelectronic technology. It shall consist of representatives of the Member States, who may be assisted by experts or advisers depending on the nature of the project under consideration, with a Commission representative as Chairman. It will meet at least twice a year.

2. The proceedings of the Committee shall be confidential.

3. The Committee shall adopt its own rules of procedure.

4. Secretarial services for the Committee shall be provided by the Commission.

ARTICLE 7

The Commission may consult the Committee on any matter falling within the scope of this Regulation including, but not limited to:

- level of detail of information to be delivered concerning national activities as specified, in article 3
- level of detail of information to be made available either publically or to Member States Government agencies
- procedures and measures to make such information available
- updating of technical specifications for projects potentially eligible for aid
- minimum number of firms required to make a project eligible for aid
- appraisal of applications and granting of aids.

ARTICLE 8

1. Where the procedure laid down in this article is to be followed, the matter shall be referred to the Committee by its Chairman, either on his own initiative, or at the request of the representative of a Member State.

2. Within the Committee, the votes of the Member States shall be weighted as provided for in article 148 (2) of the Treaty. The Chairman shall not vote.

3. The Commission representative shall submit a draft of the measures to be taken accompanied by an outline of the main elements of decision. The Committee shall give its opinion on this draft within a period to be fixed by the Chairman having regard to the urgency of the matter. It shall adopt its opinion by a majority of 45 votes.

4. The Commission shall adopt decisions which shall apply immediately. However, if these decisions are not in accordance with the Opinion of the Committee, they shall forthwith be communicated by the Commission to the Council. In that event the Commission shall defer application of the decisions which it has adopted for not more than two months from the date of such communications. The Council, acting by qualified majority, may take a different decision within two months.

ARTICLE 9

Each year the Commission shall forward to the European Parliament and to the Council a report on the development of the activities in the Community falling within the scope of this Regulation.

ARTICLE 10

The Commission, after consulting the Committee, shall adopt any supplementary measures which may be necessary for implementation of this Regulation.

ARTICLE 11

This Regulation shall enter into force on 1981

It shall apply until .....1985.

This Regulation shall be binding in its entirety and directly applicable in all Member States.

Done at Brussels,

BY THE COUNCIL
THE PRESIDENT.

TECHNICAL ANNEX TO THE PROPOSAL FOR A COUNCIL REGULATION (EEC) CONCERNING COMMUNITY ACTIONS IN THE FIELD OF MICROELECTRONIC TECHNOLOGY

Outline technical specification of projects and activities for which financial support is being proposed under the terms of the draft regulation:

I) STEP AND REPEAT ON WAFER

Direct Optical Stepping Technology

Direct optical stepping machines should be available in production with the characteristics listed below by the end of 1982, preproduction version should be delivered by the end of 1981.

- Wafer size: up to 6 inch
- Die size: 1 cm^2
- Minimum line widths: 1.25 μm on the wafer (1.1 on the resist)
- Automatic registration: 0.1 μm
- Throughput 50 x 4 inch wafers per hour at 1 cm^2 field with insertion of 5 test patterns and auto-registration at each chip; addition of a reticle magazine.

Individual times should be given in the description of the equipment including the time to insert test patterns. Registration should be programmable (per individual exposure - per block - per wafer). Minimum allowable size of alignment marks should be given.

It is considered desirable that machines could be supplied in 1983 wit an improved throughout of 50 x 6 inch wafers per hour and improved resolution of 1.0 μm minimum line width on wafer.

II) ELECTRON BEAM FOR DIRECT-WRITING ON WAFER

Electron Beam Direct Writing Equipments

E-Beam machines capable of :

- Wafer size: 6 inch
- Throughput: 15 to 20 layers/hr. at 1 μm
- Die size: no limitation
- Minimum feature size: 0.5 μm
- Spot size: variable
- Registration accuracy: 0.1 μm

This equipment should also be suitable for Reticle and Mask making. Prototype machines meeting all these requirements apart from speed must be available within 1983.

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III. PLASMA ETCHING

A. Minimum performances of the equipment

- Materials to be etched

  * SiO_2, doped and undoped

  * Si_3N_4

  * polysilicon, doped and undoped

  * silicides and polycides

  * aluminium and aluminium alloys

  * other metals for contacts and interconnections

  * organic polymers for multilevel resists and multilevel metallization

- Structures to be etched in production

  * pitch: (line plus spacing) : 3 μm

  * minimum linewidth: 1 - 1.5 μm

  * precision: + or - 10% of linewidth for the critical structures

- Selectivity and anisotropy

  The selectivity has to be adequate and for each layer it should be possible to etch completely anisotropically.

- Throughput

  The minimum throughput should be 50 wafers/hour for the slowest process. The slowest process will probably be the etching through 0.8 μm of thermal SiO_2 with a selectivity of 10:1 over Si and with a pitch of 3 μm. The etching of other layers e.g. 0.4 μm undoped polysilicon over SiO_2 should be much faster.

B. Design of the equipment

We consider a parallel plate reactor with the following features:

- Design Concept

  Most important is the use of a modular design concept so that the equipment can be optimally adapted for each application.

- Load lock

Undesired species (e.g. water vapor) should be blocked from the reaction chamber and post-etching effects must be avoided. This can be reached with a vacuum lock containing the cassettes. Stripping of the photoresist in the unload-lock should be considered as an option.

- Electrode and chamber construction

* Individually driven thermostats for upper and lower electrode and for the reaction chamber. The range for temperature control is 15-100°C standard and up to 150°C as an option.

* Electrode distance adjustable between: 5-70 mm (batch oriented system)
5-70 mm (single wafer system)

* The electrode assembly must be suited for operation at high frequencies (untill 27.12 MHz) e.g. avoid parasitic plasma anywhere in the reactor.

* Both parallel plasma etching (PE) and reactive ion etching (RIE) must be possible in the system (anode and cathode coupling).

- Vacuum design

* the region of interest is between 10 m Torr and 10 Torr

* Adjustable pumping speed

* Automatic AND manual pressure control with simple switching between the two modes.

* Use of non-corrosive materials for seals (fittings, O-rings) and tubing.

- Gas cabinet

Flexible handling of 1 to 3 gasses with 1 to 3 mass flow controllers, preferrentially extendable to 5 gasses (number of gasses is an option).

- Controls

  * The following parameters must be controllable:

    gasline(s) in use
    flowrate
    process time
    time to stabilize
    time to overetch
    R.F. power
    temperature of both electrodes
    voltage on electrode

  * The electrical signal from the sensors (pressure sensor,...) must be easily accessible (e.g. on a standard plug) for process monitoring.

  * At least one window to look into the plasma and additional flange(s) to hook up some analytical tools for process monitoring should be available.

- Software for automatic etching

  * a keyboard and necessary memory for the step by step command of the process or the maintenance sequence

  * a plug-in PROM, user programmed, for automatic etching.

- Wafer handling

  Automatic wafer handling, cassette to cassette load and unload without wafer damage or contamination.
  The system should handle wafers of 3 inch up to 150 mm diameter.

- Maintenance and safety

  * Easy dismantling for cleaning and repair

  * Standardisation of flanges, seals, plugs, etc. and spare parts.

IV) TESTING EQUIPMENT

European testers for integrated circuits should be developed with the following characteristics:

- of the integral analog/digital type

- of modular design, in order to be adaptable to both development- and production testing tasks

- development in two phases, as far as the digital part is concerned. The first step should be a tester for clock-rates of 10-20 MHz, the second step aiming at 50-100 MHz. This stepwise development has the advantage that the technological know-how, built-up in the first phase can be used to tackle the problems that have to be faced in the second development round. Moreover, the high speed test development can thus be adapted to the developing requirements of the European IC-industry in the high speed bipolar circuits.

- testing of devices with an increasing number of pins (from 64 to 128)

- substantial parts of the testsystem have to be "ECL-specific"

- testing of memory devices alone has been excluded, however "on-the-chip" memories are becoming increasingly important and therefore their testing has to be covered.

- one single high level test language concept should be supplied for the different tester configurations.

V) CAD FOR VLSI

1. Architecture

The problems to be tackled are the disciplines of specification, simulation and testing at the architectural design phase and the architectural strategies like error management and structured logic. The following activities appear to be required:

- Improvement in knowledge of computer techniques by VLSI designers through (a) transfer of know-how from computer manufacturers (b) better integration of computer science and electronic engineering training in universities.

- research on :

  (a) linking of behavioural and structural design by development of suitable languages and simulators

  (b) synthesis of logic from RTL description

  (c) error management including fault-tolerant aspects of VLSI architecture

  (d) structured logic including minimisation for PLAs (Programable Logic Arrays) and automatic programming of PLAs and ROMs (Read Only Memories)

  (e) firmware generation and simulation aids

  (f) parallel processing machines for signal processing

2. Language and Data structure

1. Design Data Management

Conventional graphic IC design systems are based upon a bottom up representation of the circuit being designed. This is considered inadequate for coping with the problems of VLSI design, and instead, a specification of a file management or design management system must be formulated with respect to the following purposes:

1) to aid the management of a large number of files representing alternative representations of many modules of a system

2) to protect the integrity of a design involving a team effort

3) to manage design modifications

4) to aid re-partitioning of a design

5) to manage the provision of design documentation

Research projects must be initiated which will enhance the normal filing system or operating system to provide the above facilities. The smallest unit of data in a transaction will be a complete file, and so conventional databases are not appropriate. The implementation must be carried out with portability in mind. A standard language must be used with well defined interfaces to standard filing systems. This project should be a joint project between IC designers, CAD tool specialists, and computer scientists.

2. User Interface

Some design activities are highly interactive and demand a guaranteed fast response from the computer while not demanding a very powerful computer. An example is design specification using graphical techniques. Such activities can be supported on a small computer dedicated to a single user. Other activities are not primarily interactive, but do require very powerful computing facilities. An example is simulation. Such activities need powerful time-shared systems.

It is important that the computers supporting these related activities should be intimately connected. Techniques for controlling tasks split between two or more computers, and for allowing flexible movement of data between these tasks, should be investigated. General principles applicable to a wide range of hardware should be established.

The present trend in hardware design specification is to use text based language descriptions which are convenient for expressing the hierarchical structure, modularity, and repetitivity which is inevitable with VLSI. However, designers still tend to think in terms of diagrams, and graphical aids will continue to be valuable in the design process. A project ought to be launched to investigate methods of combining textual and graphical representations allowing each to be converted automatically into the other, so that the most appropriate interface can be freely chosen at each part of the design process.

3. Simulation

Software tools for simulation, test and verification have to span the design spectrum from RTL-s down to transistor level. Activity should be directed towards the development of a flexible multi-level structural description language for NMOS and CMOS VLSI. Automatic compiler generation into the syntax of presently used single level tools, and, more importantly, directly into the data structure of mixed mode simulators needs investigation. Mixed mode simulation techniques need considerable attention in the area of data structures, algorithms, and models.

It is strongly recommended to pay special attention to VLSI network analysis rather than pure simulation in order to reduce design time and ensure design correctness. This is a completely new research domain which looks entirely feasable based on the data structures and algorithms of presently existing mixed mode simulators.

4. Verification

Instead of intensive verification of manually performed or interactive design steps, the goal should be to automate as much as possible (silicon compilation, standard cell technique, etc.) to make verification unnececessary. To find a solid basis for the use or creation of such tools, a study should be initiated which compares the different approaches as well as different handcrafted layouts to find objective criteria for the fundamental principles of efficiency in layout.

The hierarchical design of VLSI is obvious. The verification between the different levels of hierarchy is a problem but cannot be avoided. In spite of the hierarchy, the complexity and amount of data is enormous and with todays tools leads to uneconomic computer times. Therefore, further candidates for research and development are dedicated hardware modules (e.g. design rule checkers, pattern memory plus counters and shift registers, or hardware language processors which produce the appropriate data structures).

5. Influence of New Computer Architectures

On the basis of the assumption that:

- software is now expensive and should be optimised while hardware is cheaper and can be used more freely
- in the last few years a lot of high performance parallel processors have been developed and implemented
- the architecture of a machine should fit the problem it is to solve,

investigation in the following two areas is proposed:

1. Development of new parallel algorithms and new data structures in any CAD branch, to exploit and implement the maximum parallelism.
2. Study of new special purpose hardware processor to be interfaced with currently existing computer systems to improve part of their performance by at least one order of magnitude.

3. Testing : Summary of recommendations

The team on testing recommend to organize the future work following the three main areas and the related topics listed below :

MAIN AREA OF ACTIVITIES

	RESEARCH	SPECIFICATION & EVALUATION	DEVELOPMENT
1) TEST DATA GENERATION			
- functional level testing (methods and strategies)	*		
- element level ATPG	*		
- ATPG for LSI cells, regular logic etc.	*		
- fault types and models	*		
- fault simulation strategies	*		
- modular ATPG system		*	*
- language for MTPG		*	*
- integrated ATDG system		*	*
2) DESIGN FOR TESTABILITY			
- partitioning	*		
- RAM design for testability	*		
- microprogrammed units	*		
- design for testability general techniques	*		
- hardware implemented self testing	*		
- software/firmware self testing	*		
3) DATA ACQUISITION AND DATA MANAGEMENT			
- DADM system		*	*
- program development tools		*	*

4. Device Modeling : Summary of recommendations

The present report on Device Modeling covers three main areas :

- Numerical device simulation
- Analytical models
- Table models

For each of them, the main recommendations are summarized below.

1. Numerical device simulation

The main target of this subproject is that of stimulating European research centres and laboratories to develop advanced device-simulation packages, and make them available to European I.C. manufecturers. This should allow reaching an independence with respect to American and Japanese counterparts. The need for such an activity stems from the fact that, due to the importance of two-, and even three-dimensional effects, numerical device simulation represents the only predictive tool which can practically be used for device design.
It is therefore recommended that at least 4 simulation packages be developed, namely :

- 2-D MOSFET simulator
- 2-D simulator for bipolar devices
- 3-D MOSFET simulator
- 3-D simulator for bipolar devices

For each of them, detailed specifications have been defined concerning the physical phenomena to be incorporated in the program, the physical and geometrical device structure, and I/O graphical capabilities.

2. Analytical models (MOSFET's only)

An activity in this area is essential for two main reasons : from the one hand analytical models trading off accuracy and simplicity are mostly suited for circuit designers in CAD circuit simulation programs; on the other hand, the functional dependence of relevant electrical parameters on geometrical and physical device structure is most easily identified in analytical models, which can, therefore, provide some insight in the physical phenomena occuring within a device.
The following analytical models should be developed :

SURFACE CHANNEL MOSFET's	(Long channel, low voltage (level 1) (Long channel, high voltage (level 2) (Short channel, low voltage (level 3) (Short channel, high voltage (level 4)
BURIED CHANNEL MOSFET's	(Long channel, (level 1) (short channel, (level 2)

Physical model

Again, detailed specifications are provided for each of the above models. In addition to the development of the models, the problem of parameter identification should be tackled and solved, especially as far as charges (or capacitances) are concerned.

3. Table models

The need of table models has been recognized for timing simulation purposes. In such simulators, the capacitances are rather poorly handled, being assumed as constants; therefore, the activity in this area should aim at developing tables for both curents and capacitances. The most important problem to be solved is that of providing the scaling rules, while maintaining the computationel simplicity which is needed in order to strongly reduce the CPU time, with respect to that needed with analytical models.

COST ESTIMATES

Assuming : - 4 to 5 years worklife of the equipment

- 8 to 10 preproduction units to be delivered by one single manufacturer
- a period of trials (leased equipment) and interactive relationship between the manufacturer and the users of 18 to 24 months

including direct costs of personnel involved in the project

not including: company overheads, the cost of auxiliary facilities surrounding the equipment under development (clean room, up-stream and down-stream equipments etc.) and the training of personnel.

The following broad figures emerge (in Mio ECU):

	TOTAL GROSS COST OF THE PROJECT	PUBLIC SUPPORT
Project I : Wafer Steppers	8	4
Project II : Electron Beam	40	20
Project III : Plasma	8	4
Project IV : Testing	16	8
Project V : C.A.D.	32	16